Data Sheet December 2000 File Number 4016.5

8-Channel, 16-Bit, High Precision, Sigma-Delta A/D Sub-System

The HI7188 is an easy-to-use 8-Channel sigma-delta programmable A/D **subsystem** ideal for low frequency physical and electrical measurements in scientific, medical, and industrial applications. The subsystem has complete on-chip capabilities to support moving the intelligence from the system controller and towards the sensors. This gives the designer faster and more flexible configurability without the traditional drawbacks of low throughput per channel, higher power or cost per channel. Extreme design complexity and excessive software overhead is eliminated.

The HI7188 contains a fully differential 8 channel multiplexer, Programmable Gain Instrumentation Amplifier (PGIA), 4th order sigma-delta ADC, integrating filter, line noise rejection filters, calibration and data RAMs, clock oscillator, and a microsequencer. Communication with the HI7188 is performed via the serial I/O port, and is compatible with most synchronous transfer formats, including both the Motorola/Intersil 6805/11 series SPI, QSPI and Intel 8051 series SSR protocols.

The powerful on-board microsequencer provides automatic conversions on the multiplexed input channels (up to 8) by controlling all channel switching, filtering and calibration. The microsequencer supports on-the-fly multiplexer reconfiguration, forty to fifty times faster throughput than the competition and zero step response delay during internal or external multiplexer channel changes. A simple set of commands gives the user control over calibration, PGIA gain, and bipolar/unipolar modes on a per channel basis. Number of channels to convert, data coding, line noise rejection, etc. is programmed at the chip level. The calibration RAMs allow the user to read and write system calibration data while the data RAMs provide a read support of the conversion results for each channel.

This design is effectively eight 16-bit (for 96dB noise-free dynamic range) Sigma-Delta A/D converters combined with a microsequencer and an eight-channel multiplexer in a single package. The HI7188 provides 120dB line-noise rejection at 240 samples/second/channel (in 60Hz line-rejection mode) and 200 samples/second/channel (in 50Hz line-rejection mode) base output data rates. By reusing multiplexer channels for the same input, throughput can Fully Differential 8-Channel Multiplexer and Reference

Features

- Fully Differential 8-Channel Multiplexer and Reference
- Automatic Channel Switching with Zero Latency
- 240 Conversions Per Second Per Channel
- 16-Bit Resolution with No Missing Codes
- 0.0015% Integral Non-Linearity
- Fully Software Configurable
  - 120dB Rejection of 60/50Hz Line Noise
  - Channel Conversion Order and Number of Active Channels
  - True Bipolar or Unipolar Input Range Per Channel
  - PGIA Gain Per Channel
  - 2-Wire or 3-Wire Interface
- Chopper Stabilized PGIA with Gains of 1 to 8
- Serial Data I/O Interface, SPI Compatible
- 3 Point System Calibration
- Low Power Dissipation of 30mW (Typ)

Applications

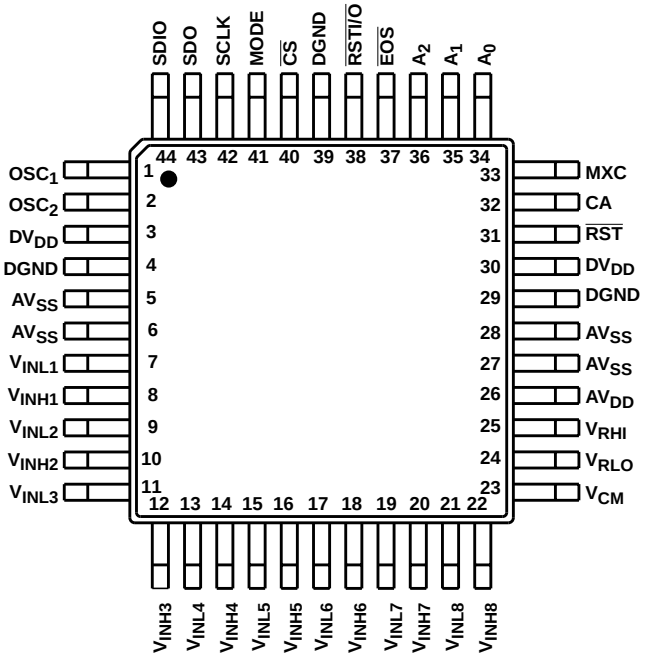
- Multi-Channel Industrial Process Controls
- Weight Scales
- Medical Patient Monitoring
- Laboratory Instrumentation
- Gas Monitoring System
- Reference Literature
  - AN9504 “A Brief Introduction to Sigma Delta Conversion”
  - TB329 “Intersil Sigma-Delta Calibration Techniques”
  - AN9518 “Using the HI7188 Evaluation Kit”
  - AN9610 “Interfacing the HI7188 to a Microcontroller”
  - AN9538 “Using the HI7188 Serial Interface

Ordering Information

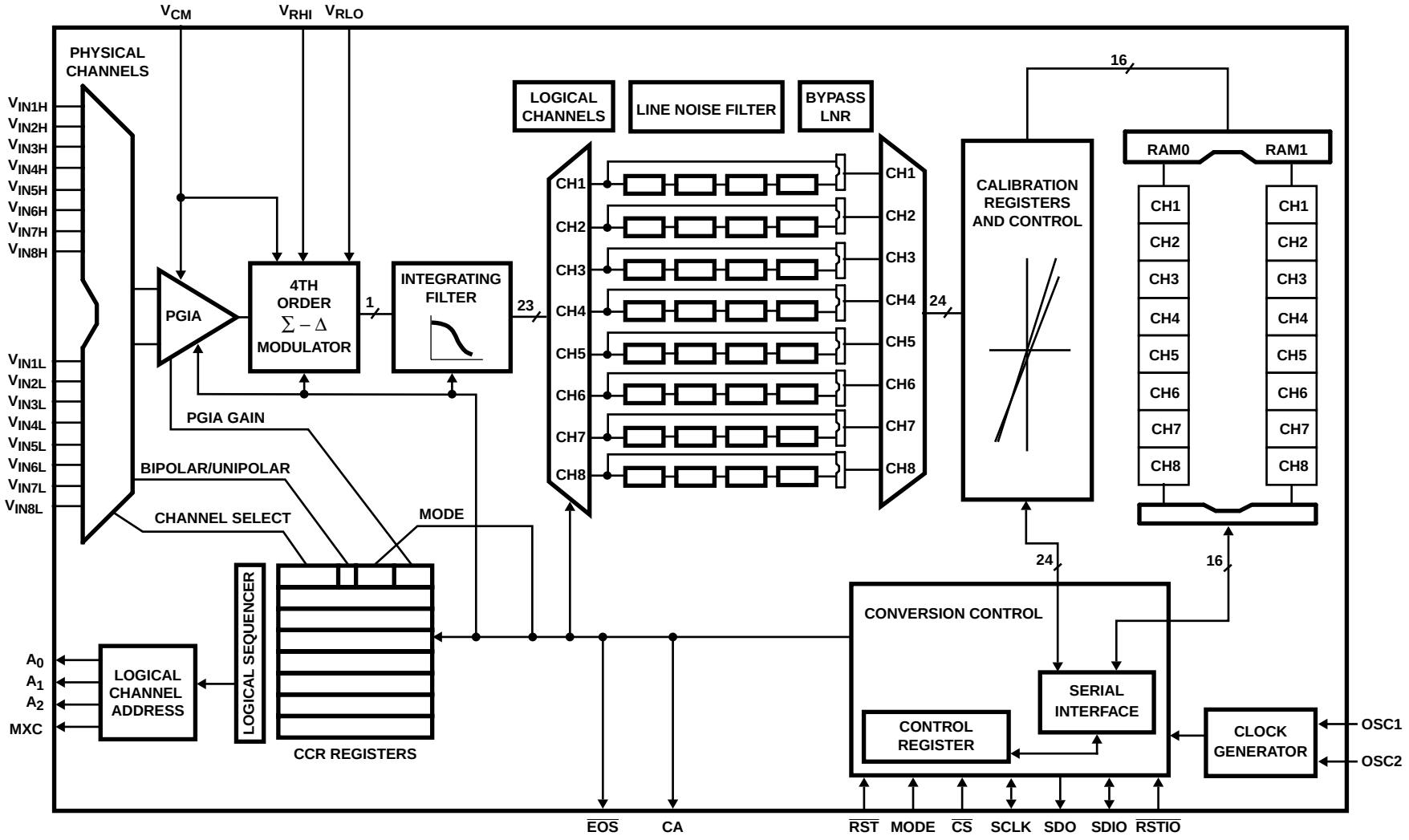
PART NUMBER	TEMP. RANGE (^{O}C)	PACKAGE	PKG. NO.
HI7188IN	-40 to 85	44 Ld MQFP	Q44.10x10
HI7188EVAL	25	Evaluation Kit	

Pinouts

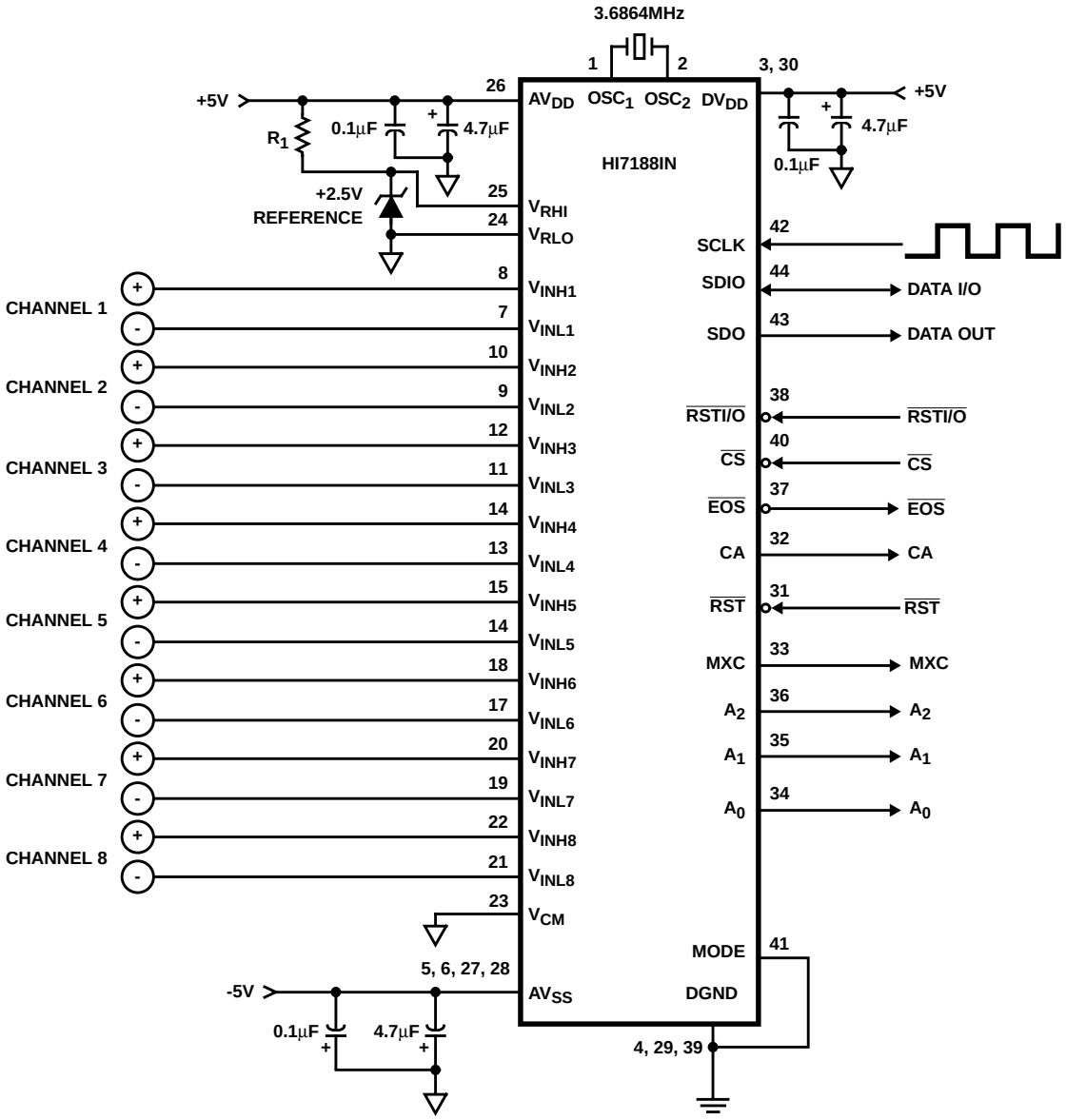
HI7188 (MQFP)
TOP VIEW



Functional Block Diagram



Typical Application Schematic



Pin Descriptions

44 LEAD MQFP	PIN NAME	PIN DESCRIPTION
41	MODE	Mode input. Used to select between Synchronous Self Clocking (MODE = 1) or Synchronous External Clocking (MODE = 0) for the Serial Port.
42	SCLK	Serial interface clock. Synchronizes serial data transfers. Data is input on the rising edge and output on the falling edge.
43	SDO	Serial Data Out. Serial data is read from this line when using a 3-wire serial protocol such as the Motorola Serial Peripheral Interface.
44	SDIO	Serial Data IN or OUT. This line is bidirectional programmable and interfaces directly to the Intel Standard Serial Interface using a 2-wire serial protocol.
1	OSC_1	Oscillator clock input for the device. A crystal connected between OSC_1 and OSC_2 will provide a clock to the device, or an external oscillator can drive OSC_1. The oscillator frequency should be 3.6864MHz to maintain Line Noise Rejection.
2	OSC_2	Used to connect a crystal source between OSC_1 and OSC_2. Leave open otherwise.
3, 30	DV_{DD}	Positive Digital supply (+5V).
4, 29, 39	DGND	Digital supply ground.
5, 6, 27, 28	AV_{SS}	Negative analog power supply (-5V).
7	V_{INL1}	Analog input low for Channel 1.
8	V_{INH1}	Analog input high for Channel 1.
9	V_{INL2}	Analog input low for Channel 2.
10	V_{INH2}	Analog input high for Channel 2.
11	V_{INL3}	Analog input low for Channel 3.
12	V_{INH3}	Analog input high for Channel 3.
13	V_{INL4}	Analog input low for Channel 4.
14	V_{INH4}	Analog input high for Channel 4.
15	V_{INL5}	Analog input low for Channel 5.
16	V_{INH5}	Analog input high for Channel 5.
17	V_{INL6}	Analog input low for Channel 6.
18	V_{INH6}	Analog input high for Channel 6.
19	V_{INL7}	Analog input low for Channel 7.
20	V_{INH7}	Analog input high for Channel 7.
21	V_{INL8}	Analog input low for Channel 8.
22	V_{INH8}	Analog input high for Channel 8.
23	V_{CM}	Common mode voltage. Must be tied to the mid point of AV_{DD} and AV_{SS}.
24	V_{RLO}	External reference input. Should be negative referenced to V_{RHI}.
25	V_{RHI}	External reference input. Should be positive referenced to V_{RLO}.
26	AV_{DD}	Positive analog power supply (+5V).
31	$\overline{RST}$	Active low Reset pin. Used to initialize modulator, filter, RAMs, registers and state machines.
32	CA	Calibration active output. Indicates that at least one active channel is in a calibration mode.
33	MXC	Multiplexer control output. Indicates that the conversion for the active channel is complete.
34	A_0	Logical channel count output (LSB).
35	A_1	Logical channel count output.
36	A_2	Logical channel count output (MSB).
37	$\overline{EOS}$	End of scan output. Signals the end of a channel scan (all active channels have been converted) and data is available to be read. Remains low until data RAM is read.
38	$\overline{RSTI/O}$	I/O reset (active low) input. Resets serial interface state machine only.
40	$\overline{CS}$	Active low chip select pin. Used to select a serial data transfer cycle. When high the SDO and SDIO pins are three-state.

Absolute Maximum Ratings

Supply Voltage
- AV_{DD} to AV_{SS} 11V
- DV_{DD} to DGND . . . . . +5.5V

Analog Input Pins. . . . . AV_{SS} to AV_{DD}
Digital Input, Output and I/O Pins . . . . . DGND to DV_{DD}
ESD Tolerance (No Damage)
- Human Body Model 500V
- Machine Model. 100V
- Charged Device Model. 500V

Thermal Information

Thermal Resistance (Typical, Note 1) θ_{JA} (^{O}C/W)
- MQFP 65

Maximum Storage Temperature Range . . . . . -65^{O}C to 150^{O}C
Maximum Junction Temperature . . . . . 150^{O}C
Maximum Lead Temperature (Soldering 10s) . . . . . 300^{O}C
(MQFP - Lead Tips Only)

Operating Conditions

Operating Temperature Range . . . . . -40^{O}C to 85^{O}C

CAUTION: Stresses above those listed in "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress only rating and operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied.

NOTE:

1. θ_{JA} is measured with the component mounted on a low effective thermal conductivity test board in free air. See Tech Brief TB379 for details.

Electrical Specifications

AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 3.6864MHz, Bipolar Input Range Selected

PARAMETER	TEST CONDITION	-40^{O}C TO 85^{O}C			UNITS
		MIN	TYP	MAX	
SYSTEM PERFORMANCE					
Resolution	Dependent on Gain (Note 2)	-	-	16	Bits
Integral Non-Linearity, INL	F_S = 25Hz, +FS, +MS, 0, -MS, -FS End Point Line Method (Notes 3, 5, 6)	-	±0.0015	±0.0045	%FS
Differential Non-Linearity	(Note 2)	No Missing Codes to 16-Bits			-
Offset Error, V_{OS} (Calibrated)	$V_{INHI} = V_{INLO}$ (Notes 3, 4)	-	±0.0015	-	%FS
Full Scale Error, FSE (Calibrated)	$V_{INHI} - V_{INLO}$ = +2.5V (Notes 3, 4)	-	±0.0015	-	%FS
Gain Error (Calibrated)	Slope = +Full Scale - (-Full Scale) (Notes 3, 4)	-	±0.0015	-	%FS
Noise, $V_{N(P-P)}$		-	1/4	-	LSB
Common Mode Rejection Ratio, CMRR	V_{CM} = 0V (Note 5) Delta V_{CM} = ±3V	-	-75	-	dB
Off Channel Isolation	(Note 2)	-120	-	-	dB
ANALOG INPUT					
Common Mode Input Range, V_{CM}	(Note 2)	AV_{SS}	-	AV_{DD}	-
Input Leakage Current, I_{IN}	$V_{IN} = AV_{DD}$ (Note 3)	-	-	1.0	nA
Input Capacitance, C_{IN}	(Note 2) See Table 2	-	4.0	-	pF
DIGITAL INPUTS					
Input Logic High Voltage, V_{IH}		2.0	-	-	V
Input Logic Low Voltage, V_{IL}		-	-	0.8	V
Input Logic Current, I_I	V_{IN} = 0V, +5V	-	1.0	10	µA
Input Capacitance, C_{IN}	V_{IN} = 0V (Note 2)	-	5.0	-	pF
DIGITAL CMOS OUTPUTS					
Output Logic High Voltage, V_{OH}	I_{OUT} = -100µA (Note 7)	2.4	-	-	V
Output Logic Low Voltage, V_{OL}	I_{OUT} = 3.2mA (Note 7)	-	-	0.4	V
Output Three-State Leakage Current, I_{OZ}	V_{OUT} = 0V, +5V (Note 7)	-	1	10	µA
Digital Output Capacitance, C_{OUT}	(Note 2)	-	10	-	pF

Electrical Specifications AV_{DD} = +5V, AV_{SS} = -5V, DV_{DD} = +5V, V_{RHI} = +2.5V, V_{RLO} = AGND, V_{CM} = AGND, PGIA Gain = 1, OSC_{IN} = 3.6864MHz, Bipolar Input Range Selected **(Continued)**

PARAMETER	TEST CONDITION	-40°C TO 85°C			UNITS
		MIN	TYP	MAX	
TIMING CHARACTERISTICS					
SCLK Minimum Cycle Time, t_{SCLK}	(Notes 2, 7)	200	-	-	ns
SCLK Minimum Pulse Width, t_{SCLKPW}	(Notes 2, 7)	60	-	-	ns
$\overline{CS}$ to SCLK Precharge Time, t_{PRE}	(Notes 2, 7)	50	-	-	ns
Data Setup to SCLK Rising Edge (Write), t_{DSU}	(Notes 2, 7)	50	-	-	ns
Data Hold from SCLK Rising Edge (Write), t_{DHLD}	(Notes 2, 7)	0	-	-	ns
Data Read Access from Instruction Byte Write, t_{ACC}	(Notes 2, 7)	-	-	40	ns
Read Bit Valid from SCLK Falling Edge, t_{DV}	(Notes 2, 7)	-	-	40	ns
Last Data Transfer to Data Ready Inactive, $t_{\overline{DRDY}}$	(Notes 2, 7)	-	50	-	ns
$\overline{RESET}$ Low Pulse Width t_{RESET}	(Notes 2, 7)	100	-	-	ns
$\overline{RSTI/O}$ Low Pulse Width $t_{\overline{RSTI/O}}$	(Notes 2, 7)	100	-	-	ns
MUX High Pulse Width t_{MUX}	(Notes 2, 7)	14	-	-	µs
CADDR Valid to MUX High	(Notes 2, 7)	-	-	75	ns
Oscillator Clock Frequency	(Notes 2, 7)	-	3.6864	-	MHz
Output Rise/Fall Time	(Notes 2, 7)	-	-	30	ns
Input Rise/Fall Time	(Notes 2, 7)	-	-	1	µs
POWER SUPPLY CHARACTERISTICS					
IAV_{DD}	AV_{DD} = +5V, OSC_1 = 3.6864MHz (Note 3)	-	1.8	3.0	mA
IAV_{SS}	AV_{SS} = -5V, OSC_1 = 3.6864MHz (Note 3)	-	1.8	3.0	mA
IDV_{DD}	DV_{DD} = +5V, SCLK = 4MHz	-	2.0	4.0	mA
Power Dissipation, Active PD_A	AV_{DD} = +5V, AV_{SS} = -5V, SLP = '0' (Notes 3, 9)	-	28	50	mW
Power Dissipation, Sleep PD_S	AV_{DD} = +5V, AV_{SS} = -5V, SLP = '1' (Notes 3, 9)	-	5	-	mW
PSRR (ΔV_{supply} = 0.25V)	PSRR = 20log (ΔV_{supply} / ΔV_{OS}) (Note 3)	-	75	-	dB

NOTES:

2. Parameter guaranteed by design or characterization, not production tested.
3. DC PSRR is measured on all supplies individually and applies to both Bipolar and Unipolar Input Ranges.
4. These errors can be removed by re-calibrating at the desired operating temperature.
5. Applies after system calibration.
6. Fully differential input signal source is used.
7. See Load Test Circuit, Figure 1, R_1 = 10kΩ, C_L = 50pF (Includes Stray and Jig Capacitance).
8. For Line Noise Rejection, 3.6864MHz is required to develop internal clocks to reject 50/60Hz.
9. SLP is the sleep mode enable bit defined in bit 3 of the Control Register (CR <3>).

Test Circuits

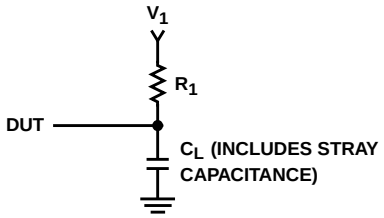
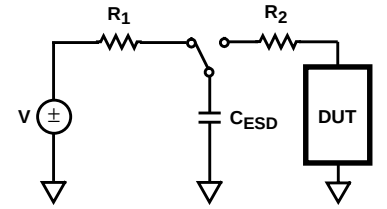


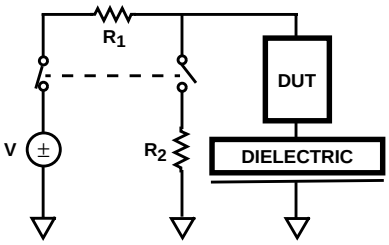
FIGURE 1. LOAD TEST CIRCUIT



HUMAN BODY
C_{ESD} = 100pF
R_1 = 10MΩ
R_2 = 1.5kΩ

MACHINE MODEL
C_{ESD} = 200pF
R_1 = 10MΩ
R_2 = 0Ω

FIGURE 2. HUMAN BODY AND MACHINE MODEL ESD TEST CIRCUIT



CHARGED DEVICE MODEL
R_1 = 1GΩ
R_2 = 1Ω

FIGURE 3. CHARGE DEVICE MODEL ESD TEST CIRCUIT

Waveforms

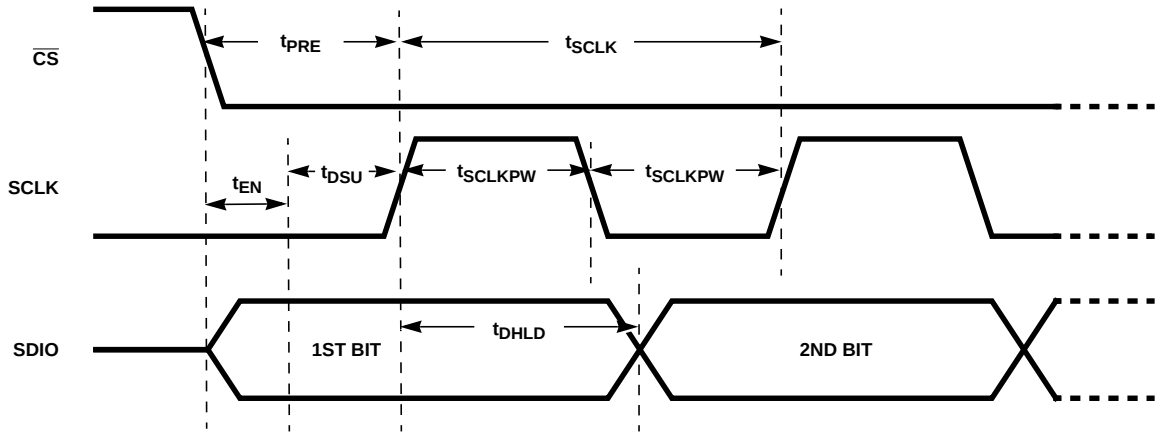


FIGURE 4. DATA WRITE TO HI7188

Waveforms (Continued)

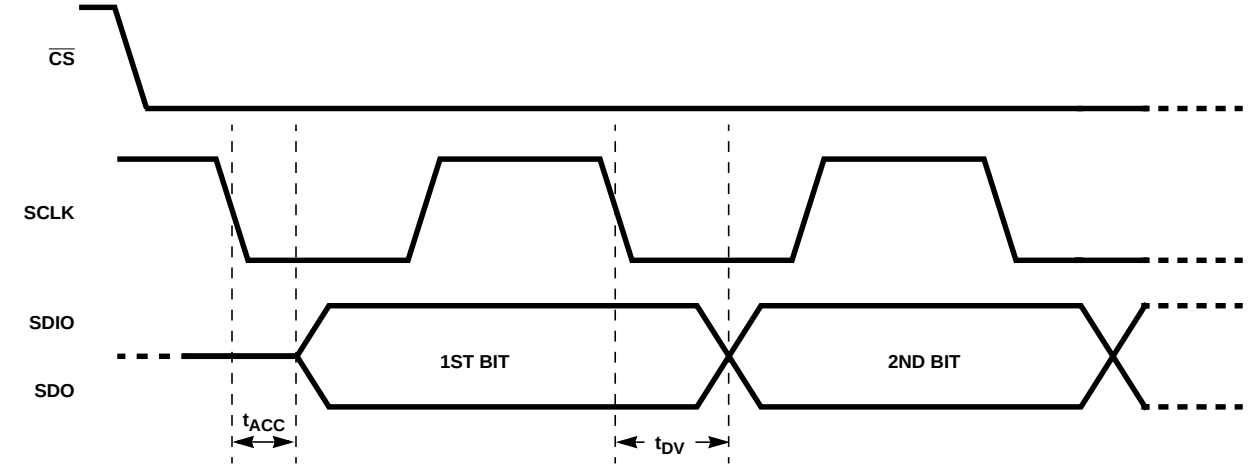


FIGURE 5. DATA READ FROM HI7188

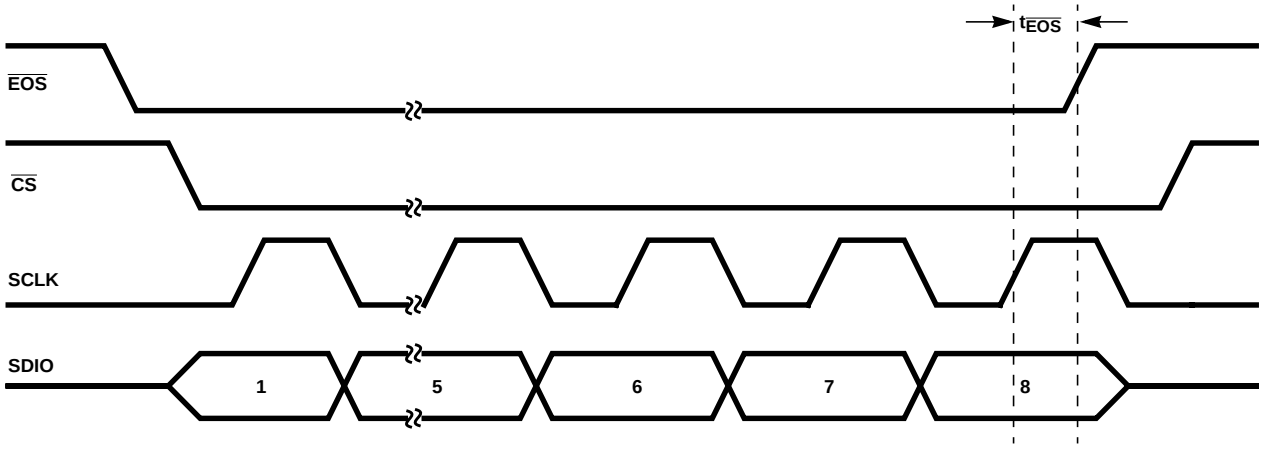


FIGURE 6. DATA READ FROM HI7188

Definitions

Integral Non-Linearity (INL) - This is the maximum deviation of any digital code from a straight line passing through the endpoints of the transfer function. The endpoints of the transfer function are zero scale (a point 0.5 LSB below the first code transition 000...000 and 000...001) and full scale (a point 0.5 LSB above the last code transition 111...110 to 111...111).

Differential Non-Linearity (DNL) - This is the deviation from the actual difference between midpoints and the ideal difference between midpoints (1 LSB) for adjacent codes. If this difference is equal to or more negative than 1 LSB, a code will be missed.

Offset Error (V_{OS}) - The offset error is the deviation of the first code transition from the ideal input voltage (V_{IN} - 0.5 LSB).

Full Scale Error (FSE) - The full scale error is the deviation of the last code transition from the ideal input full-scale voltage (V_{IN}- + V_{REF}/Gain - 1.5 LSB).

Input Span - The input span defines the minimum and maximum input voltages the device can handle while still calibrating properly for gain.

End of Scan (EOS) - The end of scan is a signal used to indicate all active logical channels have been converted and data is available to be read.

Line Noise Rejection - Line noise rejection is the ability to attenuate (reject) signals at the frequency of power lines typically 50Hz or 60Hz.

Physical/Logical Channel - A physical channel pertains to channels which are directly connected to the device package pins identified in the pinout. Logical channels are predefined in the Channel Configuration Registers (CCR) with a physical channels reference (address) being made by the user. Refer to the Channel Configuration Registers section for examples.

Functional Description

The HI7188 contains a differential 8 channel multiplexer, Programmable Gain Instrumentation Amplifier (PGIA), 4th order sigma-delta ADC, integrating filter, line noise rejection filters, Calibration and data RAMs, bidirectional serial port, clock oscillator, and a microsequencer. The 8 to 1 multiplexer at the input combined with the resetable modulator on the HI7188 allow for conversions of up to 8 differential channels with each channel being updated at a rate of 240 samples per second (with 60Hz line noise rejection enabled). The device can be programmed for conversion of any combination of physical channels. After the signal has passed through the multiplexer, it moves into the PGIA. The PGIA can be configured in gains of 1, 2, 4 and 8 specific for each of the 8 logical channels. The signal then enters the sigma delta modulator. The patented one-shot sigma delta modulator is a fourth order modulator which converts the differential analog signal into a series of one bit outputs. The 1's density of this data stream provides a digital representation of the analog input. The output of the modulator is fed into the integrating low pass digital filter. Data out of the filter is available after 201 bits are received from the modulator.

If the device is in line noise rejection mode, the integrating filter data is routed to the Line Noise Rejection filters. This data is then calibrated using the offset and gain calibration coefficients. Data coding is performed and the result is stored in the data RAM. If line noise rejection is disabled, the averaging filter is bypassed, calibration is performed on the data from the integrating filter, the data is coded, and the result is stored in the data RAM.

This data flow of modulation, filter and calibrate is repeated for each of the active logical channels (up to 8). After all active logical channels are converted the HI7188 generates an active low interrupt, End Of Scan ($\overline{EOS}$), that indicates all logical channels have been updated and valid data is available to be read from the data RAM.

Converted data is read via the HI7188 serial I/O port which is compatible with most synchronous transfer formats including both the Motorola SPI and Intel 8051 series SSR protocols. All RAMs, including the Data RAM, are accessed in a "burst" mode. That is, the data for all active logical channels is accessed in a single read communication cycle.

Using the HI7188

This section describes how to use the device for a typical application. This includes power supply considerations, initial reset, calibration and conversion. Please refer to Figure 7.

The analog and digital supplies and grounds are separate on the HI7188 to minimize digital noise coupling into the analog circuitry. Nominal supply voltages are AV_{DD} = +5V, DV_{DD} = +5V, and AV_{SS} = -5V. If the same supply is used for AV_{DD} and DV_{DD} it is imperative that the supply is separately decoupled to the AV_{DD} and DV_{DD} pins on the HI7188. Separate analog and digital ground planes should be maintained on the system board and the grounds should be tied together back at the power supply.

When the HI7188 is powered up it needs to be reset by pulling the $\overline{RST}$ line low. This resets the internal registers as shown in Table 1. This initial configuration defines the part for one active logical channel (physical channel 1, address 000), conversion mode, unipolar operation, gain of one, no line noise rejection, offset binary coding, MSB first I/O bit order, descending I/O byte order, and single line interface. After the $\overline{RST}$ line returns high, the device immediately begins converting as described above without any further instruction. There is no correction for offset or gain errors on the converted data at this time. To ensure maximum performance, calibration should be done as defined in the operation mode section.

TABLE 1. REGISTER RESET VALUES

REGISTER	VALUE (HEX)
Data Output Registers	XXXX (undefined)
Channel Configuration Register #2	00XXXXXX
Channel Configuration Register #1	XXXXXXXX
Control Register	0000
Offset Calibration Registers	000000
Positive Full Scale Calibration Registers	800000
Negative Full Scale Calibration Registers	800000

The reset configuration should be updated to reflect the users system including chip level and channel level programming.

1. Chip level refers to programming common to all channels such as 50/60 Hertz Line Noise Rejection, number of active channels, etc. and is detailed in the Control Register (CR) section.
2. Channel level programming is custom for each channel such as gain, physical input and mode as detailed in the Channel Configuration Registers (CCR) section.

A calibration routine should be performed next to remove system offset and full scale errors (see Calibration section). The CCR is used to place each channel of the device in several operational modes including Conversion, System Offset Calibration, System Positive Full Scale Calibration and System Negative Full Scale Calibration. Each channel inputs should be connected and settled to the correct input condition before the CCR is programmed for each calibration point. After a complete system calibration is performed, the desired analog input is applied and accurate data can be read via the serial interface. The device should be recalibrated when there is a change in the user configuration (i.e. gain, unipolar/bipolar), supply voltage or ambient temperature.

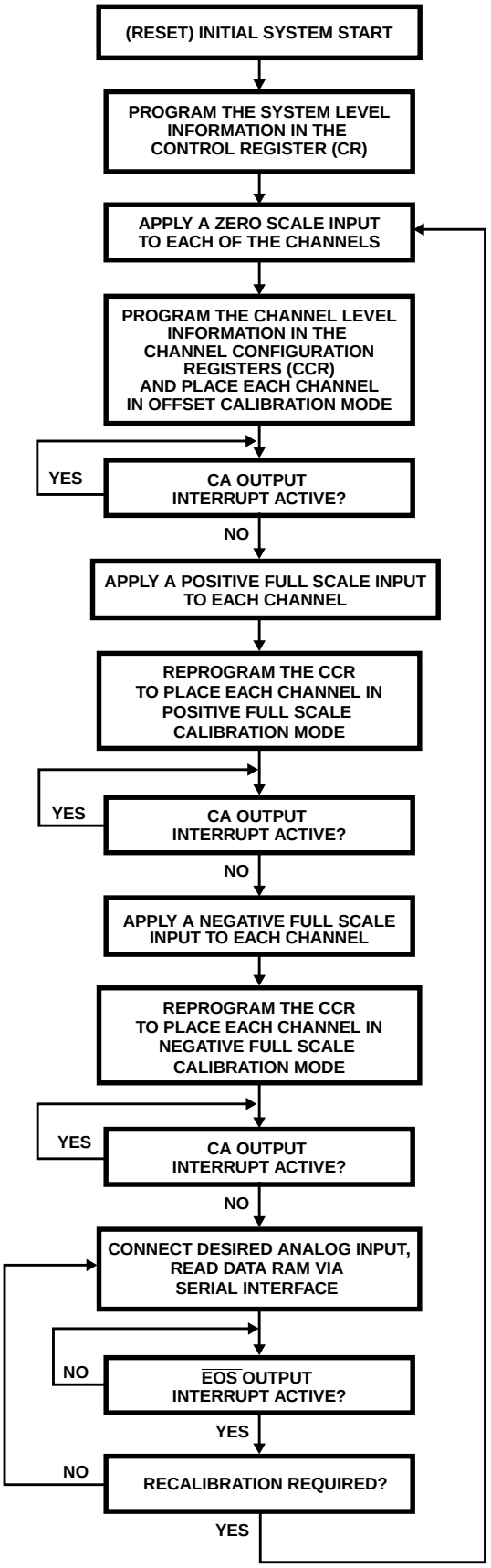


FIGURE 7. SYSTEM USAGE FLOWCHART

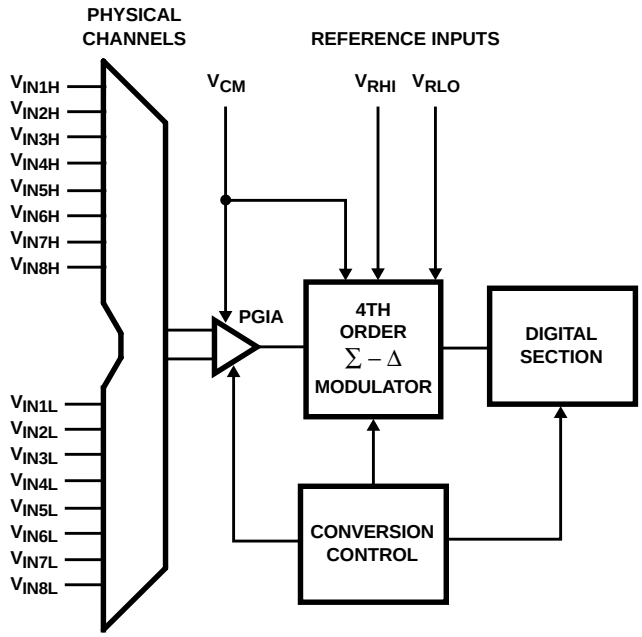


FIGURE 8. ANALOG BLOCK DIAGRAM

The configuration can be saved by writing the contents of the CR, CCR and calibration RAMs to microprocessor system memory (see Serial Interface section). After this has occurred, the configuration can easily be restored back to the HI7188 in the event of power failure or reset.

Analog Section Description

The analog portion of the HI7188 consists of a 8 to 1 fully differential Multiplexer, Programmable Gain Instrumentation amplifier (PGIA) and a 4th order Sigma-Delta modulator. Please refer to the simplified analog block diagram in Figure 8.

Analog Inputs

The analog inputs on the HI7188 are fully differential inputs with programmable gain capabilities. The inputs accept both unipolar and bipolar input signals and gains of 1, 2, 4 or 8. The gain for any given physical channel is independent of the gain of other physical channels. The gain is programmed via the Channel Configuration Register (CCR).

The input impedance of the HI7188 is dependent upon the modulator input sampling capacitors which varies with the selected PGIA gain. Table 2 shows the sampling capacitors and input impedances for the different gain settings of the HI7188. Note that this table is valid only for a 3.6864MHz master clock. If the input clock frequency is changed then the input impedance will change accordingly. The equation used to calculate the input impedance is

$$Z_{IN} = 1/(C_S \times F_S)$$

Where C_S is the internal sampling capacitance and F_S is the modulator sampling rate set by the master clock divided by six (F_S = 3.6864MHz/6 = 614.4kHz).

TABLE 2. EFFECTIVE INPUT IMPEDANCE vs GAIN

GAIN	SAMPLING RATE (kHz)	SAMPLING CAPACITOR (pF)	INPUT IMPEDANCE (kΩ)
1	614.4	4	407
2	614.4	8	203
4	614.4	16	102
8	614.4	32	51

Bipolar/Unipolar Input Ranges

The inputs can accept either unipolar or bipolar input voltages with each physical channel's mode being independent of other physical channels. Bipolar or unipolar options are chosen by programming the bipolar/unipolar (B/$\overline{U}$) bits of the Channel Configuration Registers (CCR). Programming the logical channels for either unipolar or bipolar operation does not change any of the input signal conditioning. The inputs are differential, and as a result are referenced to the voltage on the V_{INL} input. For example, if V_{INHX} is +3.75V and logical channel X is configured for unipolar operation with a gain of 1 and a V_{REF} of +2.5V, the input voltage range on the V_{INLX} input is +1.25V to +3.75V. If V_{INLX} is +1.25V and logical channel X is configured for bipolar mode with gain of 1 and a V_{REF} of +2.5V, the analog input range on the V_{INHX} input is -1.25V to +3.75V.

Multiplexer

The input multiplexer is a fully differential 8 channel device controlled by the internal microsequencer. Any number of inputs, up to 8, can be scanned and both the number of physical channels scanned and the scanning order are controlled by the users programming of the Channel Configuration Register (CCR). The output of the multiplexer feeds the input to the Programmable Gain Instrumentation Amplifier (PGIA).

External Multiplexers

For interfacing the HI7188 to external multiplexers several output pins are available. These pins include MXC, A_2, A_1 and A_0. Refer to Figure 9. The MXC pulse is active high during the modulator and integrating filter reset pulse. The pulse width is typically 14.6µs with LNR disabled and 54.6µs with LNR enabled. This signal can be used to "break before make" an external multiplexer. Referring to Figure 9, the data conversion time involves the actual input channel A/D conversion while the calibration time involves data calibration and coding of the conversion results. The address pins A_2, A_1 and A_0 describe the **logical** address which is currently being converted. The user can utilize these output pins to drive external multiplexer address pins.

The main critical issue is the external multiplexer output must switch and settle to 0.00153% (16 bits) of the final value during the MXC reset pulse and prior to Data Integration or data errors will occur. The input must be stable only during the data integration period but can be changed during the calibration period.

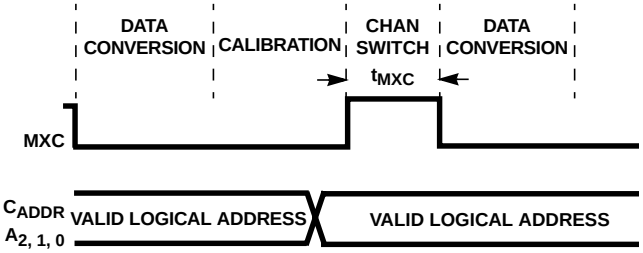


FIGURE 9. CHANNEL SWITCHING TIMING

Programmable Gain Instrumentation Amplifier

The Programmable Gain Instrumentation Amplifier (PGIA) allows the user to interface low level sensors and bridges directly to the HI7188. The PGIA has 4 selectable gain options of 1, 2, 4, and 8. The gain of each physical channel is independent of other physical channels and is programmable by writing the G1 and G0 bits in the Channel Configuration Registers (CCR).

Differential Reference Input

The reference inputs, V_{RHI} and V_{RLO}, provide a differential reference input capability. V_{RHI} must always be greater than V_{RLO} for proper operation of the device. The common mode range for these differential inputs is from AV_{SS} to AV_{DD} and the nominal differential voltage ($V_{REF} = V_{RHI} - V_{RLO}$) is +2.5V. Larger values of V_{REF} can be used with minor degradation in performance. Smaller values of V_{REF} can also be used but performance will be degraded since the system noise is larger relative to the LSB size. The full scale range of the HI7188 is defined as:

$$FSR_{BIPOLAR} = 2 \times V_{REF}/GAIN$$

$$FSR_{UNIPOLAR} = V_{REF}/GAIN$$

The reference inputs provide a high impedance dynamic load similar to the analog inputs. For proper circuit operation these pins must be driven by low impedance circuitry. Reference noise outside of the band of interest will be removed by the digital filter but excessive reference noise inside the band of interest will degrade performance.

V_{CM} Input

The V_{CM} input is the internal reference voltage for the HI7188 analog circuitry and should always be tied to the midpoint of the AV_{DD} and AV_{SS} supplies. This point provides a common mode input voltage for the internal operational amplifiers and must be driven from a low noise, low impedance source if it is not tied to analog ground. Failure to do so will result in degraded HI7188 performance.

It is recommended that V_{CM} be tied to analog ground when operating off of AV_{DD} = +5V and AV_{SS} = -5V supplies. V_{CM} also determines the headroom at the upper and lower ends of the power supplies which is limited by the common mode input range where the internal operational amplifiers remain in the linear, high gain region of operation.

Sigma Delta Modulator

The sigma delta modulator is a fourth order modulator which converts the differential analog signal into a series of one bit outputs. The 1's density of this data stream provides a digital representation of the analog input. Figure 10 shows a simplified block diagram of the analog modulator front end of a Sigma-Delta A/D Converter. The input signal V_{IN} comes into a summing junction (the PGIA in this case) where the previous modulator output is subtracted from it. The resulting signal is then integrated and the output of the integrator goes into the comparator. The output of the comparator is then fed back via a one bit DAC to the summing junction. The feedback loop forces the average of the fed back signal to be equal to the input signal V_{IN}.

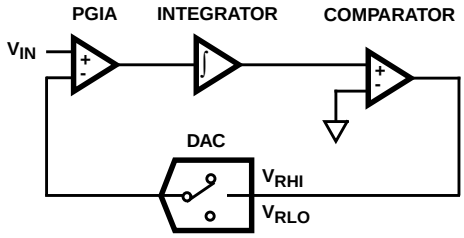


FIGURE 10. SIMPLE MODULATOR BLOCK DIAGRAM

Digital Section Description

A block diagram of the digital section of the HI7188 is shown in Figure 11. This section includes an integrating filter, averaging filters, calibration logic registers, output data RAM, digital serial interface and a clock generator.

Integrating Filters

The integrating filter receives a stream of 1s and 0s from the modulator at a rate of 614kHz. The 1's density of this data stream provides a digital representation of the analog input signal. The integrating filter provides the low pass function with a cutoff of 2kHz. The Integrating Filter works in concert with the modulator and is controlled by the same clock and reset signals. The filter integrates 201 1-bit samples from the modulator for a valid "conversion" to be completed. At that time the data is transferred to the Line Noise Rejection (LNR) Filters or straight to calibration if LNR is not selected.

Line Noise Rejection

The line noise rejection section is used to eliminate a periodic sine wave signal of either 50Hz or 60Hz line frequencies.

To understand the functionality of the HI7188 line noise rejection (LNR), it is useful to discuss the method utilized by a generic integrating analog to digital converter (ADC). This ADC uses an external summing/integrating capacitor to sum the line noise on a capacitor over one line noise cycle. The cycle period is 16.67ms and 20ms for 60Hz and 50Hz respectively. The ADC output is then the desired input with the line noise summed to zero with a conversion rate equal to the line noise frequency.

The HI7188 has the ability to do the same function as the Integrating ADC but samples the input **four** times during the line cycle (see Figure 12). For this discussion, the desired analog input signal will be zero. The HI7188 accomplishes this by instituting a four quadrant, four point running average system. The microsequencer samples all eight inputs at exactly the same point in time and for the exact amount of time for each of the four quadrants of a single line cycle and stores them separately. These four samples are then summed, on a per channels basis, which results in the same answer of the line synchronous noise as with the Integrating ADC.

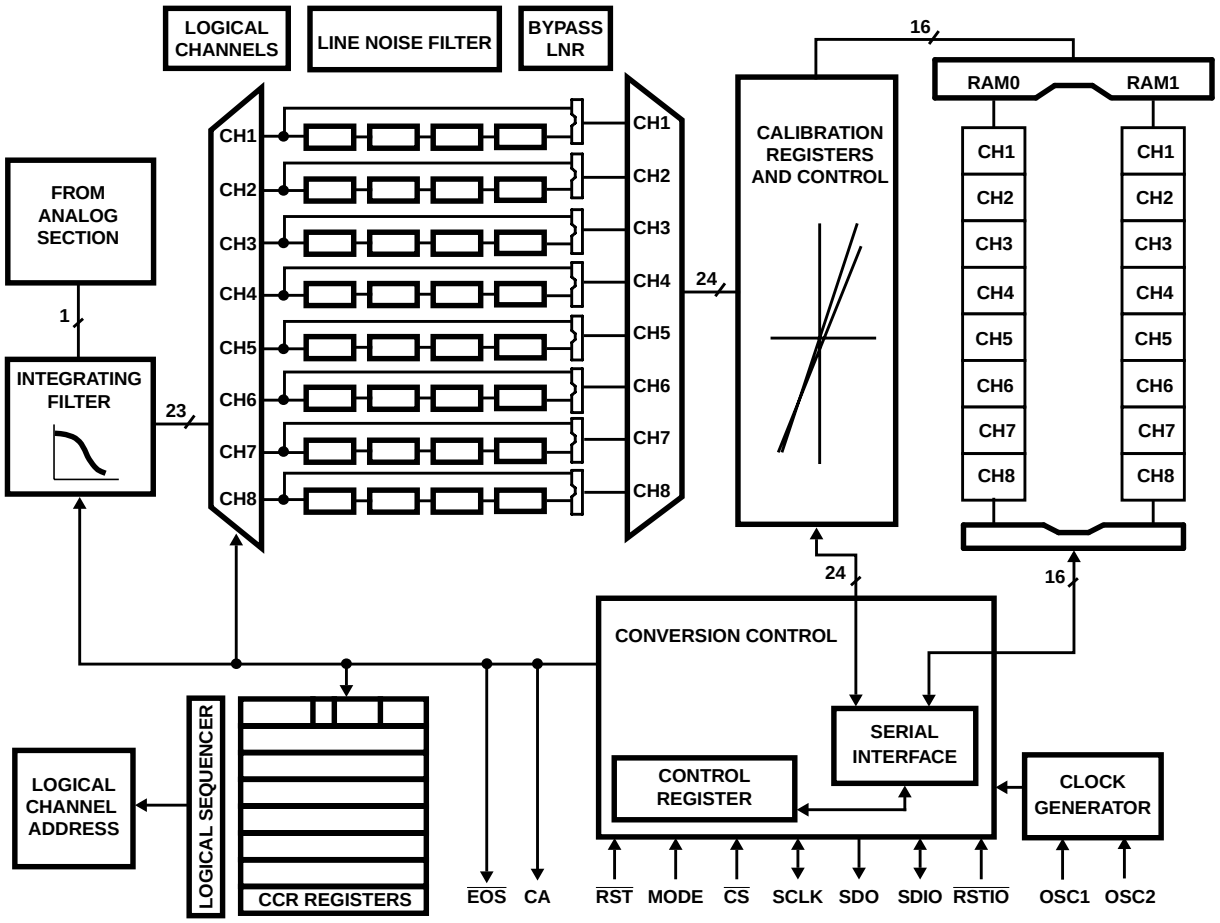


FIGURE 11. DIGITAL BLOCK DIAGRAM

A one channel example:

1. Channel 1 is sampled four times as labeled S1, S2, S3, and S4 in Figure 12. One sample for each 90 degrees quadrant of line cycle (quarter main cycle).
2. Each sample is equally spaced (From zero, S1 = 5 degrees, S2 = 95 degrees, S3 = 185 degrees and S4 = 275 degrees).
3. Each sample is of the same duration of time.
4. Samples S1 and S3 (180 degrees later) will have the equal magnitudes of line noise but have opposite signs.
5. Samples S2 and S4 (180 degrees later) will have the equal magnitudes but opposite signs.
6. The HI7188 sums the samples S1, S3, S2 and S4 which results in averaging the line noise signal to zero.
7. These four samples are placed, real time, in the 4x8 array of registers used for LNR. The next quadrant sampled (S5) replaces S1 in the running average. The new sample replaced S1 at the same point on the line cycle, 5 degrees but 360 degrees later. The line noise summation is still zero. Now for every quarter main cycle thereafter, the LNR will be updated and line noise free output will be available.

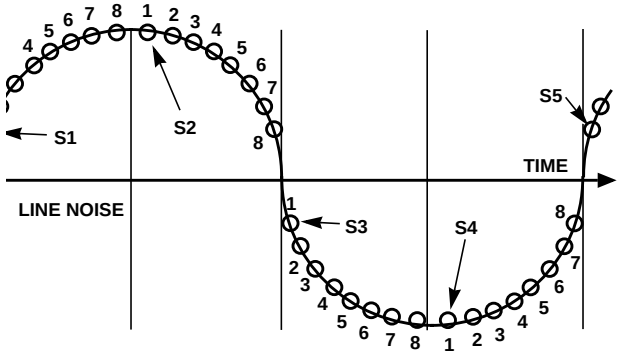


FIGURE 12. LINE NOISE CYCLE INCLUDING PATENTED TIME SPACED INPUT SAMPLING

Calibration

Calibration is the process of adjusting the conversion data based on known system offset and gain errors. For a complete system calibration to occur, the on-chip microcontroller must perform a three point calibration which involves recording conversion results for three different input conditions - “zero-scale,” “positive full-scale,” and “negative full-scale”. With these readings, the HI7188 can null any system offset errors and calculate the positive and negative gain slope factors for the transfer function of the system. It is

imperative that the zero-scale calibration be performed before either of the gain calibrations. The order of the gain calibrations is not important. Non-calibrated data can be obtained from the device by writing 000000 (h) to the Offset Calibration Register, 800000 (h) to the Positive Full Scale Calibration Register, and 800000 (h) to the Negative Full Scale Calibration Register. This sets the offset of the part to 0 and both the positive and negative gain slope factors to 1.

A calibration routine should be initiated whenever there is a change in the ambient operating temperature or supply voltage. It should also be initiated if there is a change in the gain, bipolar, or unipolar input range.

The user may choose to ignore data during calibration or check whether any ACTIVE channel is in calibration. Bit 12, the SE bit, of the Control Register offers capability to suppress the $\overline{EOS}$ interrupt during calibration. If the SE bit is high the $\overline{EOS}$ interrupt will be suppressed if any active logical channel is in the calibration mode. If the SE bit is high and no active logical channels are in the calibration mode the $\overline{EOS}$ interrupt will function normally. If low, the suppress $\overline{EOS}$ function is disabled. To check whether any logical channel is in calibration the user can monitor the Calibration Active (CA) output pin. The CA output pin is high when at least one of the active logical channels are in calibration. If a non active logical channel is in calibration the CA will not be high. The user can monitor the CA pin to determine when all active logical channels are calibrated.

NOTE: When the user accesses the calibration RAMs, via the Serial Interface, the conversion process stops, resetting the modulator, integrating filter and clearing the $\overline{EOS}$ interrupt. When the calibration RAM I/O operation is completed the device automatically restarts beginning on logical channel 1. The contents of the CR and CCR are not affected by this I/O.

Calibration Time

The calibration time varies depending several factors including LNR (50Hz/60Hz) being enabled or disabled, and 2 point calibration. Table 3 contains a summary of the conversion time depending on these factors. Since line noise rejection is a major factor this discussion is divided accordingly.

TABLE 3. CALIBRATION TIME

LNR	LNR FREQ (Hz)	ACTIVE CHANS	CAL PNTS	EACH CAL POINT (ms)	TOTAL CAL (ms)
On	50	n/a	2	20	40
On	50	n/a	3	20	60
On	60	n/a	2	16.7	33.3
On	60	n/a	3	16.7	50.0
Off	n/a	N	2.5 2	N (0.4803)	2N (0.4803)
Off	n/a	N	3	N (0.4803)	3N (0.4803)

NOTE: N is the number of active channels. Total Cal column assumes zero switching time between calibration points.

Line Noise Rejection On

When line noise rejection is enabled, it takes 4 conversion scan periods to fill the averaging filters used for attenuating the periodic line noise. A conversion scan involves converting all 8 logical channels at a rate dependent on whether LNR is set to 50Hz or 60Hz. The scan period is 5ms (1/200Hz) and 4.167ms (1/240Hz) respectively. The number of active channels is not applicable in this calculation since the microsequencer converts on ALL logical channels to maintain LNR timing regardless of the number of user defined active channels.

Line Noise Rejection Off

Operation of the device is altered slightly when LNR is disabled. Since the microsequencer is not synchronizing for any line noise, the conversion rate increases to 260.3 conversions second/channel (10% increase). With LNR disabled, a conversion scan involves converting only the ACTIVE logical channels. When ACTIVELY converting on less than 8 channels, this is the major speed advantage over LNR enabled which sets conversion scan period based on ALL eight logical channels. Refer to Table 3.

System Offset Calibration

The system offset calibration mode is a process that allows the user to lump offset errors of external circuitry and the internal errors of the HI7188 together and null them out. This mode will convert the external differential signal applied to the V_{IN} inputs and then store that value in the offset calibration RAM for that physical channel. To invoke the system offset calibration the user applies the “zero scale” voltage to the physical channel requiring calibration, then writes the related CCR byte indicating offset calibration is required. The next time this logical channel is converted, the microsequencer performs calibration and updates the related offset RAM. Next the internal microsequencer places that logical channel back into the conversion mode and updates the CCR byte.

System Positive Full Scale Calibration

The system positive full scale calibration mode is a process that allows the user to lump positive gain errors of external circuitry and the internal gain errors of the HI7188 together to calculate the positive transfer function of the system. This mode will convert the external differential signal applied to the V_{IN} inputs and then store that value in the system positive full Scale calibration RAM for that physical channel. To invoke the system positive full scale calibration the user applies the “positive full scale” voltage to the physical channel requiring calibration, then writes the related CCR byte indicating positive full scale calibration is required. The next time this logical channel is converted, the microsequencer performs calibration and updates the related system positive full scale calibration RAM. Next the internal microsequencer places that logical channel back into the conversion mode and updates the CCR byte.

System Negative Full Scale Calibration

The system negative full scale calibration mode is a process that allows the user to lump negative gain errors of external circuitry and the internal gain errors of the HI7188 together to calculate the negative transfer function of the system. This mode will convert the external differential signal applied to the VIN inputs and then store that value in the system negative full scale calibration RAM for that physical channel. To invoke the system negative full scale calibration the user applies the "negative full scale voltage", which must be equal to Vref, to the physical channel requiring calibration, then writes the related CCR byte indicating negative full scale calibration is required (see note below). The next time this logical channel is converted, the microsequencer performs calibration and updates the related system negative full scale calibration RAM. Next the internal microsequencer places that logical channel back into the conversion mode and updates the CCR byte.

TEMPORARY NOTE: In bipolar mode, the user MUST perform negative full scale calibration with the exact differential voltage applied to the Vref pins, otherwise large errors will occur at the zero crossing point. During normal conversions, the error occurs when the input is at the offset calibration point. At this point, plus or minus 1/2 LSB, the output code will be either the true half scale reading of 7FFF/8000 (offset binary coding) or negative full scale 0000.

Offset and Gain Adjust Limits

Whenever a calibration mode is used, there are limits to the amount of offset and gain which can be adjusted. For both bipolar and unipolar modes the minimum and maximum input spans are 0.2 x V_{REF}/GAIN and 1.2 x V_{REF}/GAIN respectively. In the unipolar mode the offset plus the span cannot exceed the 1.2 x V_{REF}/GAIN limit. So, if the span is at its minimum value of 0.2 x V_{REF}/GAIN, the offset must be less than 1 x V_{REF}/GAIN. In bipolar mode the span is equidistant around the voltage used for the zero scale point. For this mode the offset plus half the span cannot exceed 1.2 x V_{REF}/GAIN. If the span is at ±0.2 x V_{REF}/GAIN, then the offset can not be greater than ±2 x V_{REF}/GAIN.

Range Detection

In addition to the calibration process, the converter detects over range above positive full scale and under range below minus full scale conditions. Over or under range detection affects the output data coding as described in the Data Coding section.

Over range detection is identical for both bipolar and unipolar operation. Over range is detected by comparing the offset corrected filter output to the positive gain coefficient. If the current offset corrected filter value is greater than the positive gain coefficient, an over range condition is detected.

In unipolar mode, under range is detected by sampling the sign bit of the offset calibrated data. If the sign bit is logic 1, signifying a negative voltage, an under range condition exists.

In bipolar mode, under range is detected by comparing the offset corrected filter output to the negative gain coefficient. If the current offset corrected filter value is less than the negative gain coefficient, an under range condition is detected.

Data Coding

The calibrated data can be obtained in one of various numerical codes depending on the bipolar/unipolar mode bit and the two's complement coding bit. In bipolar mode, if the two's complement bit is high, the output is two's complement. In bipolar mode, offset binary coding is used when the two's complement coding bit is low. In unipolar mode, only binary coding is available and the two's complement coding bit is a don't care.

The output coding for the HI7188 is shown in Tables 4 and 5. V_{ZS} represents the applied zero scale input during system offset calibration. V_{PFS} represents the applied positive full scale input during system positive full scale calibration. V_{NFS} represents the applied negative full scale input during system negative full scale calibration.

TABLE 4. BIPOLAR MODE OUTPUT CODES (HEX)

INPUT VOLTAGE	TWO'S COMPLEMENT CODE	OFFSET BINARY CODE
>(V_{PFS} - 1.5 LSB)	7FFF	FFFF
V_{PFS} - 1.5 LSB	7FFF/7FFE	FFFF/FFFE
V_{ZS} - 0.5 LSB	0000/FFFF	8000/7FFF
V_{NFS} + 0.5 LSB	8001/8000	0001/0000
<(V_{NFS} + 0.5 LSB)	8000	0000

TABLE 5. UNIPOLAR MODE DATA OUTPUT CODES (HEX)

INPUT VOLTAGE	BINARY CODE
>(V_{PFS} - 1.5 LSB)	FFFF
V_{PFS} - 1.5 LSB	FFFF/FFFE
V_{PFS}/2 - 0.5 LSB	8000/7FFF
V_{ZS} + .5 LSB	0001/0000
<(V_{ZS} + 0.5 LSB)	0000

When the range detection logic determines an over range, the converter output will clamp at the >(V_{PFS} - 1.5 LSB) output as described in Tables 4 and 5. When the range detection logic determines an under range, the converter output will clamp at the <(V_{NFS} + 0.5 LSB) output described in Table 4 or the <(V_{ZS} + 0.5 LSB) output described in Table 5.

Data RAM

The Data RAM block is comprised of two 8 x 16 memory elements which store conversion results after calibration and data coding. Two RAMs are required to allow a one channel scan buffer per logical channel. The user can only READ from the data RAM. For illustration, these elements are labeled

RAM0 and RAM1. The RAMs are configured such that when one is internally writable the other is readable via serial I/O. The following paragraphs describe the data RAM operation. Please refer to the Functional Block Diagram.

For example, from initialization, RAM0 is writable, RAM1 is readable, $\overline{EOS}$ is inactive. Conversion completes on all active logical channels (RAM0 stores conversion N data) and the $\overline{EOS}$ interrupt is generated. Internally, the microsequencer switches RAM0 to readable, RAM1 to writable. The user can read the data RAM to obtain N conversion results, clearing the $\overline{EOS}$ interrupt.

The next conversion N+1 completes on all active logical channels (RAM1 stores N+1 data). If a data RAM (RAM0 containing N data) read has been completed before the N+1 conversion scan has completed, RAM1 will switch to being readable and RAM0 is writable. This is normal operation and no conversion results are lost.

If the data RAM (RAM0 containing N data) is not completely read before the N+1 conversion is completed, there are two possible results.

1. The data RAM read has not been started (RAM0 containing N data), EOS remains active low and the microsequencer will switch RAM1 to be readable and RAM0 to be writable. This has the effect of overwriting conversion N with N+2.
2. The data RAM (RAM0 containing N data) read has been started but is not complete, the read pointer remains with RAM0 and the write pointer remains with RAM1. This has the effect of overwriting conversion N+1 with N+2 before N+1 can be read, therefore conversion N+1 is lost.

Clocking/Oscillators

The master clock of the HI7188 can be supplied by either a crystal connected between the OSC_1 and OSC_2 pins as shown in Figure 13A or a CMOS compatible clock signal connected to the OSC_1 pin as shown in Figure 13B and floating the OSC_2 pin. The master clock is used by the internal clock generator to derive the clock edges required for both analog and digital sections. The HI7188 is designed or a 3.6864MHz clock to maintain Line Noise Rejection.

Crystal Operation

Using a crystal to generate the clock, care must be taken to minimize any external stray capacitance/inductance seen by the OSC_1 and OSC_2 pins. If care is not taken, the feedback (crystal) loop noise will result in a non reliable master clock, which in turn, will produce erroneous conversion results. The crystal should be connected as close to the HI7188 device as physically possible. If you cannot meet these requirements, we would recommend you use an External CMOS Clock instead of the crystal.

External CMOS Clock Operation

When driving the HI7188 with an external CMOS clock, the clock should never be turned off. If the clock is turned off, the device should be re-synchronized by resetting either manually via the RESET pin or by the following special software instructions. If the device is not re-synchronized erroneous conversion results may be observed. The hardware reset will clear all registers and RAMs as defined in the data sheet. The software reset is achieved by either performing an I/O access of any calibration RAM or cycling the device through a sleep cycle.

Calibration RAM Access

To re-synchronize the conversion process the user may perform an I/O access of any calibration RAM (read or write). When the user performs this I/O access the microsequencer stops the conversion process, resets the modulator, digital filter and waits until the I/O is complete. After the I/O is completed the microsequencer automatically restarts the conversion process.

Sleep Cycle

Another method to re-synchronize the conversion process is to cycle the device through a sleep cycle. The user places the device in SLEEP mode by writing the SLP bit (CR<3>) of the Control Register to logic one. The microsequencer will stop the conversion process, reset the conversion pointer to logical channel one, clear the four line noise rejection filters and deactivate $\overline{EOS}$. The serial interface, calibration/data RAMs, CR and CCR are not affected.

To return from sleep mode the user changes the SLP bit from high to low. This restarts the conversion process beginning with logical channel 1. If line noise rejection (LNR) is enabled, it takes four complete scans (all eight channels) to refill the four line noise rejection filters before an $\overline{EOS}$ interrupt. If LNR is not enabled, it takes one conversion scan of only the active channels before an $\overline{EOS}$ interrupt. Recalibration is not required since the calibration RAMs are not effected by the sleep operation.

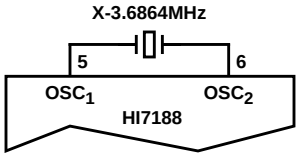


FIGURE 13A. CRYSTAL OPERATION

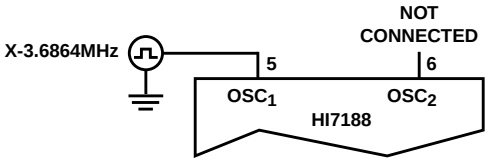


FIGURE 13B. EXTERNAL CMOS CLOCK OPERATION

Serial Interface

The HI7188 has a flexible, synchronous serial communication port to allow easy interfacing to most industry standard microcontrollers and microprocessors. The serial I/O is compatible with most synchronous transfer formats, including both the Motorola 6805/11, SPI and Intel 8051 SSR protocols. The interface supports 2-wire transfers of reading and writing on a single bidirectional line (SDIO) or 3-wire transfers of writing on SDIO and reading on the SDO line.

The Interface allows read/write access to the Control Register, Channel Configuration Registers, and Calibration RAMs. The interface allows read only access to the data RAM (refer to Table 7). The interface is byte organized with each register byte having a specific address. Single or multiple byte transfers are supported. In addition, the interface allows flexibility as to the byte and bit access order. That is, the user can specify MSB/LSB first bit positioning and can access bytes in ascending/descending order from any byte position.

Serial Interface Clock

The HI7188 supports two serial interface clock (SCLK) modes for all interface timing. This allows the greatest flexibility for different types of systems where the HI7188 can act either as master in the system (it provides the serial interface clock) or as slave (an external clock is provided to the HI7188). These two modes are defined as self clocking and external clocking respectively. Regardless of the clocking mode selected, all data is registered into the HI7188 on the rising edge of the SCLK while all data is driven out on the falling edge of SCLK. The HI7188 interface is designed to work with clock stalling in either high or low state. The clock mode is determined by the logic level applied to the MODE pin.

Synchronous Self Clocking

The device in a self-clocking scheme if the MODE pin is high. This defines the SCLK pin as an output which provides the serial clock signal used for the transfer of all data to and from the HI7188. This self-clocking mode can be used with processors which allow an external device to clock their serial port. The frequency of SCLK is one eighth of the external crystal connected between the OSC_1 and OSC_2 pins. The HI7188 is designed for a 3.6864MHz crystal which sets SCLK to 460.8kHz.

Synchronous External Clocking

The HI7188 is in a external clocking scheme if the MODE pin is low. This defines the SCLK pin as an input and an external clock must be provided to the SCLK pin. This external clocking mode is designed for direct interface to systems which provide a serial clock output which is synchronized to the serial data output. The maximum frequency of the external SCLK is 5MHz.

Burst RAM Access

The Data RAM, System Offset calibration RAM, System Positive Full Scale Calibration RAM and System Negative Full Scale Calibration RAM can **only** be accessed in a continuous RAM “Burst”. RAM burst transfers are special instructions that perform a continuous data transfer for all bits of that RAM. That is, individual bytes of any RAM cannot be accessed without reading all of the bytes. See Table 7. Each transfer occurs such that the first word transferred corresponds to the first logical channel converted as specified in the Channel Configuration Register (CCR). The first byte transferred for each word is controlled by the RB bit of the instruction byte and the bit position is determined by the Control Register (CR) MSB/LSB bit. The number of words transferred is specified by the CR bits that describe the number of logical channels being converted as well as the size of the destination RAM. This transfer mode reduces the overhead of multiple IR writes as compared to individual byte access. The following two examples are useful in understanding the RAM burst transfer instructions.

Example 1. The physical channel conversion order as specified by the CCRs is 8, 2, 3, 4, 5, 6, 1, 7. The HI7188 is setup via the Control Register to convert 8 logical channels. The IR byte written is 0xx11100 (read the data RAM). The following occurs: After completing the IR write, 16 bytes of data will be transferred from the HI7188. The first byte transferred will be the most significant byte of the physical channel 8 conversion results. The second byte will be the least significant byte of the physical channel 8 conversion results. This pattern of most significant byte followed by least significant byte will repeat, in order for physical channels 2, 3, 4, 5, 6, 1, 7.

Example 2. The physical channel conversion order as specified by the CCRs is 8, 2, 3, 4, 5, 6, 1, 7. The HI7188 is setup via the Control Register to convert only 3 logical channels. The IR byte written is 1xx01101 (write the offset RAM). The following occurs: After completing the IR write, 9 bytes of data will be written to the offset RAM (recall that the Offset Calibration register is 3 bytes wide). The first byte is the least significant byte used for offset calibration of physical channel 8. The second byte will be the middle byte used for offset calibration of physical channel 8. The third byte will be the most significant byte used for offset calibration of physical channel 8. This pattern of least significant byte to most significant byte will repeat for all logical channels converted in the logical channel order as described above. For example, the last byte transferred will be the most significant byte of physical channel 3 used for offset calibration.

NOTE: When the user accesses the calibration RAMs, via the Serial Interface, the conversion process stops, resetting the modulator, integrating filter and clearing the $\overline{EOS}$ interrupt. When the calibration RAM I/O operation is completed the device automatically restarts beginning on logical channel 1. The contents of the CR and CCR are not affected by this I/O.

Detailed Register Descriptions

Instruction Register

The instruction register is an 8 bit register which is used during a communications cycle for setting up read/write operations. Below are the bit assignments.

INSTRUCTION REGISTER (BYTE)

MSB	6	5	4	3	2	1	LSB
$\overline{R}$/W	**NB1**	**NB0**	**RB**	**A3**	**A2**	**A1**	**A0**

$\overline{R}$/W - Bit 7 of the Instruction Byte determines whether phase 2 of the communication cycle will be a read or write operation. If $\overline{R}$/W is logic 1, a write transfer will occur in phase 2 of the communication cycle. If $\overline{R}$/W is logic 0, a read transfer will occur in phase 2 of the communication cycle.

NB1, NB0 - Bits 6 and 5 of the Instruction Byte determine the number of bytes that will be transferred during phase 2 of a communication cycle, if a register is selected for I/O access. If a RAM is selected for IO access, these bits are don't care. Any number of bytes from 1 to 4 is allowed. See Tables 6 and 7.

TABLE 6. MULTIPLE BYTE ACCESS BITS

NB1, NB0 IR [6:5]	DESCRIPTION
00	Transfer 1 Byte
01	Transfer 2 Bytes
10	Transfer 3 Bytes
11	Transfer 4 Bytes

RB - Bit 4 is used to determine the byte order when accessing a RAM address. When accessing a RAM address, if RB = 1, the data format is most significant byte first to least significant byte. When accessing a RAM address, if RB = 0, the data format is least significant byte first to most significant byte. When accessing a register address, this bit is a don't care.

A3, A2, A1, A0 - Bits 3 and 2 (A3 and A2) of the Instruction Byte determine which of the three internal registers will be accessed or if both bits are set (11b), that a RAM access is active. For register addresses, bits 1 and 0 (A1 and A0) determine which byte of that register will be accessed first. For RAM access (A3 = 1, A2 = 1), bits 1 and 0 (A1 and A0) determine which RAM is the source or destination.

TABLE 7. INTERNAL REGISTER ADDRESS

$\overline{R}$/W IR [7]	NB1, NB0 IR [6:5]	A3, A2, A1, A0 IR [3:0]	DESCRIPTION
0/1	00	0000	CR, start byte 0, 1 byte transfer
0/1	01	0000	CR, start byte 0, 2 byte transfer
0/1	00	0001	CR, start byte 1, 1 byte transfer
0/1	01	0001	CR, start byte 1, 2 byte transfer
0/1	00	0100	CCR #1, start byte 0, 1 byte transfer
0/1	00	0101	CCR #1, start byte 1, 1 byte transfer

TABLE 7. INTERNAL REGISTER ADDRESS (Continued)

$\overline{R}$/W IR [7]	NB1, NB0 IR [6:5]	A3, A2, A1, A0 IR [3:0]	DESCRIPTION
0/1	00	0110	CCR #1, start byte 2, 1 byte transfer
0/1	00	0111	CCR #1, start byte 3, 1 byte transfer
0/1	01	0100	CCR #1, start byte 0, 2 byte transfer
0/1	01	0101	CCR #1, start byte 1, 2 byte transfer
0/1	01	0110	CCR #1, start byte 2, 2 byte transfer
0/1	01	0111	CCR #1, start byte 3, 2 byte transfer
0/1	10	0100	CCR #1, start byte 0, 3 byte transfer
0/1	10	0101	CCR #1, start byte 1, 3 byte transfer
0/1	10	0110	CCR #1, start byte 2, 3 byte transfer
0/1	10	0111	CCR #1, start byte 3, 3 byte transfer
0/1	11	0100	CCR #1, start byte 0, 4 byte transfer
0/1	11	0101	CCR #1, start byte 1, 4 byte transfer
0/1	11	0110	CCR #1, start byte 2, 4 byte transfer
0/1	11	0111	CCR #1, start byte 3, 4 byte transfer
0/1	00	1000	CCR #2, start byte 0, 1 byte transfer
0/1	00	1001	CCR #2, start byte 1, 1 byte transfer
0/1	00	1010	CCR #2, start byte 2, 1 byte transfer
0/1	00	1011	CCR #2, start byte 3, 1 byte transfer
0/1	01	1000	CCR #2, start byte 0, 2 byte transfer
0/1	01	1001	CCR #2, start byte 1, 2 byte transfer
0/1	01	1010	CCR #2, start byte 2, 2 byte transfer
0/1	01	1011	CCR #2, start byte 3, 2 byte transfer
0/1	10	1000	CCR #2, start byte 0, 3 byte transfer
0/1	10	1001	CCR #2, start byte 1, 3 byte transfer
0/1	10	1010	CCR #2, start byte 2, 3 byte transfer
0/1	10	1011	CCR #2, start byte 3, 3 byte transfer
0/1	11	1000	CCR #2, start byte 0, 4 byte transfer
0/1	11	1001	CCR #2, start byte 1, 4 byte transfer
0/1	11	1010	CCR #2, start byte 2, 4 byte transfer
0/1	11	1011	CCR #2, start byte 3, 4 byte transfer
0	xx	1100	Data RAM burst transfer, least significant byte first, READ ONLY
0	xx	1100	Data RAM burst transfer, most significant byte first, READ ONLY
0/1	xx	1101	Offset RAM burst transfer, least significant byte first.
0/1	xx	1101	Offset RAM burst transfer, most significant byte first.
0/1	xx	1110	Positive full scale RAM burst transfer, least significant byte first.
0/1	xx	1110	Positive full scale RAM burst transfer, most significant byte first.
0/1	xx	1111	Negative full scale RAM burst transfer, least significant byte first.
0/1	xx	1111	Negative full scale RAM burst transfer, most significant byte first.

Control Register

The Control Register (CR) is 16 bits wide and contains information that determines operating mode and the system/chip level configuration. This configuration applies to all logical channels and cannot be modified at the channel level. Following are the bit assignments:

CONTROL REGISTER BYTE 1

MSB	14	13	12	11	10	9	LSB
T3	**T2**	**T1**	**$\overline{\text{CHOP}}$**	**SE**	**LNR**	**FS**	**TC**

CONTROL REGISTER BYTE 0

MSB	6	5	4	3	2	1	LSB
N2	**N1**	**N0**	**TP**	**SLP**	**BD**	**$\overline{\text{MSB}}$**	**SDL**

T3, T2, T1 - Bits 15, 14 and 13 are reserved and MUST always be logic zero for normal operation. These bits are low after $\overline{\text{RESET}}$ is applied.

$\overline{\text{CHOP}}$. Bit 12 is the active low chop bit used to determine whether the chopper stabilized amplifier is used or bypassed. This bit is low (chop on) after $\overline{\text{RESET}}$ is applied.

SE. Bit 11 is the active high suppress $\overline{\text{EOS}}$ bit. If high, the $\overline{\text{EOS}}$ interrupt will not go active when any logical channel is in calibration mode. If this bit is high and no logical channels are in the calibration mode, or this bit is low, $\overline{\text{EOS}}$ functionality is as previously described. This bit allows the user to suppress false $\overline{\text{EOS}}$ interrupts during calibration. Only logical channels that are actively being converted are considered. That is, if only two logical channels are being converted but the CCR byte for a non active logical channel is in a calibration mode, the $\overline{\text{EOS}}$ functionality is active. This bit is low (suppress $\overline{\text{EOS}}$ off) after $\overline{\text{RESET}}$ is applied.

LNR. Bit 10 is the active high line noise rejection (LNR) bit. If high LNR is selected. This bit is low (LNR off) after $\overline{\text{RESET}}$ is applied.

FS. Bit 9 is the 50Hz/60Hz frequency select bit. If bit 9 is high, the clock generation logic synchronizes conversions for proper rejection of 50Hz line noise. If bit 9 is low, the clock generation logic synchronizes conversions for proper rejection of 60Hz line noise. This bit is low (60Hz LNR) after $\overline{\text{RESET}}$ is applied.

TC. Bit 8 is the active high two's complement bit used to select between 2's complementary and offset binary data coding for bipolar mode. In bipolar mode, a high selects two's complement; when low data is offset binary. Note that in unipolar mode the binary data coding is not affected by the TC bit. This bit is low (offset binary data) after RESET is applied.

N2, N1, N0. Bits 7, 6 and 5 are the bits that specify the number of active logical channels to be converted. See Table 8. These bits are low (one active channel) after RESET is applied.

TABLE 8. NUMBER OF CONVERSION CHANNELS

N2, N1, N0 CR [7:5]	NUMBER OF CHANNELS TO CONVERT
000	1
001	2
010	3
011	4
100	5
101	6
110	7
111	8

TP - Bit 4 is the active high two point calibration bit. When high, the positive gain slope factor is used for both positive and negative voltages. This bit is low (normal three point cal) after $\overline{\text{RESET}}$ is applied.

SLP - Bit 3 is the active high sleep mode bit used to put the device in a low power/standby mode. When high, conversion stops and the conversion pointer is reset to logical channel 1. The four line noise rejection filters are cleared and $\overline{\text{EOS}}$ is deactivated. The serial interface, calibration/data RAMs, CR and CCR are not affected.

To return from sleep mode the user changes this bit from high to low. This restarts the conversion process beginning with logical channel 1. If line noise rejection is enabled, it takes four complete scans (all active channels) to refill the four line noise rejection filters before an $\overline{\text{EOS}}$ interrupt. If line noise rejection not enabled, it takes 1 complete scan before an $\overline{\text{EOS}}$ interrupt.

This bit is low (sleep mode off) after $\overline{\text{RESET}}$ is applied.

BD. Bit 2 is the byte direction bit used to determine either ascending or descending order access for multi-byte transfers. When high, ascending order is enabled. When low, descending order is enabled. This bit is low (descending order) after $\overline{\text{RESET}}$ is applied.

$\overline{\text{MSB}}$. Bit 1 bit direction bit used to select whether a serial data transfer is MSB or LSB first. When low, MSB first mode is enabled while high selects LSB first. This bit is low (MSB first) after $\overline{\text{RESET}}$ is applied.

SDL. Bit 0 selects a two-wire or three-wire transfer protocol of the serial interface. When low, two-wire data transfers are done using the SDIO pin. Both data in and out of the part is uses the by-directional SDIO pin. When high, three-wire data transfers are done using the SDIO and SDO pins. Data into the part uses the SDIO pin while data out uses the SDO pin. This bit is low (two-wire, SDIO exclusively) after $\overline{\text{RESET}}$ is applied.

Channel Configuration Registers

The HI7188 Channel Configuration Registers (CCR) comprise a 64-bit memory element that defines the logical channel conversion order as well as each logical channel specific data such as physical channel address, mode, gain, and

bipolar/unipolar operation. The 64 bits are divided into two 32 bit register blocks referred to as CCR#2 and CCR#1. Each register contains four bytes pertaining to four logical channels. The register may be accessed 1, 2, 3 or 4 bytes at a time. Please refer to Table 10 to determine physical address assignments within the CCR and Table 9 for logical channel assignment. The physical channel conversion order is defined based on it's location in the CCR blocks. For example, if the CCR #2 <31:24> is set with the CCR <2:0> = 100, then physical channel 5 will be converted first. The CCR is byte wide accessible via the Serial Interface allowing the user to change the individual logical channel configuration on the fly. Following are the bit assignments.

TABLE 9. CHANNEL CONFIGURATION REGISTER

BLOCK	BIT LOCATION	DESCRIPTION
CCR #2	<31:24>	1st Logical Channel
CCR #2	<23:16>	2nd Logical Channel
CCR #2	<15:8>	3rd Logical Channel
CCR #2	<7:0>	4th Logical Channel
CCR #1	<31:24>	5th Logical Channel
CCR #1	<23:16>	6th Logical Channel
CCR #1	<15:8>	7th Logical Channel
CCR #1	<7:0>	8th Logical Channel

CHANNEL CONFIGURATION REGISTER (BYTE)

MSB	6	5	4	3	2	1	LSB
CH2	**CH1**	**CH0**	**B/$\overline{U}$**	**MD1**	**MD0**	**G1**	**G0**

CH2, CH1, CH0 - Bits 7, 6, 5 of the channel configuration byte determine which physical inputs are used as shown in Table 10.

TABLE 10. ACTIVE CHANNEL DECODE

CH2, CH1, CH0 CCR [2:0]	PHYSICAL INPUT PINS
000	V_{INH1}, V_{INL1}
001	V_{INH2}, V_{INL2}
010	V_{INH3}, V_{INL3}
011	V_{INH4}, V_{INL4}
100	V_{INH5}, V_{INL5}
101	V_{INH6}, V_{INL6}
110	V_{INH7}, V_{INL7}
111	V_{INH8}, V_{INL8}

B/$\overline{U}$ - Bit 4 of the channel configuration byte determine bipolar or unipolar mode. If Logic 1, bipolar mode is selected while logic 0 selects unipolar mode.

MD1, MD0 - Bit 3 and 2 of the channel configuration byte are the channel Mode bits. This defines the mode of operation for that logical channel, please see Table 11. All calibration modes automatically return to conversion mode after calibration is complete.

TABLE 11. HI7188 OPERATIONAL MODES

MD1	MD0	OPERATIONAL MODE
0	0	Conversion
0	1	System Offset Calibration
1	0	System Positive Full Scale Calibration
1	1	System Negative Full Scale Calibration

G1, G0 - Bit 1 and 0 defines the PGIA gain of 1, 2, 4 or 8. Please refer to Table 12.

TABLE 12. CHANNEL GAIN

G1, G0 CCR [1:0]	PGIA CHANNEL GAIN
00	1
01	2
10	4
11	8

Serial Interface Pin Description

The serial I/O port is a bidirectional port which is used to read and write the internal registers. The port contains two data lines, a synchronous clock, and two status flags. Figure 14 shows a diagram of the serial interface lines.

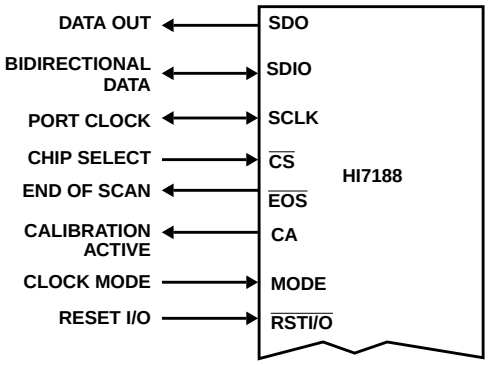


FIGURE 14. HI7188 SERIAL INTERFACE

SDO - Serial Data Out. Data is read from this line using those protocols with separate lines for transmitting and receiving data. An example of such a standard is the Motorola Serial Peripheral Interface (SPI) using the 68HC05 and 68HC11 family of microcontrollers, or other similar processors. In the case of using bidirectional data transfer on SDIO, the SDO does not output data and is set in a high impedance state.

SDIO. Serial Data In or Out. Data is always written to the device on this line. However, this line can be used as a bidirectional data line. This is done by properly setting up the Control Register. Bidirectional data transfer on this line can be used with Intel standard serial interfaces (SSR, Mode 0) in MCS51 and MCS96 family of microcontrollers, or other similar processors.

SCLK. Serial Clock. The serial clock pin is used to synchronize data to and from the HI7188 and to run the port state machines. In Synchronous External Clock Mode, SCLK is configured as an input, is supplied by the user, and can run up to a 5MHz rate. In Synchronous Self Clocking Mode, SCLK is configured as an output and runs at $OSC_1/8$ = 460.8kHz.

$\overline{CS}$. Chip Select. This signal is an active low input that allows more than one device on the same serial communication lines. The SDO and SDIO will go to a high impedance state when this signal is high. If driven high during any communication cycle, that cycle will be suspended until $\overline{CS}$ reactivation. Chip select can be tied low in systems that maintain control of SCLK.

$\overline{EOS}$. End Of Scan. Signals the end of a logical channel scan (all programmed logical channels have been converted) and data is available for reading. $\overline{EOS}$ is useful as an edge or level sensitive interrupt signal to a microprocessor or microcontroller. $\overline{EOS}$ low indicates that new data is available and the Data RAM can be read. $\overline{EOS}$ will return high upon completion of a complete Data RAM read cycle. Please refer to the Data RAM section for details.

CA. Calibration Active. This pin is high if any active logical channel is in the calibration mode and stays high for the entire scan period. CA checks only those channels that are actively being converted on. For example, if the HI7188 is programmed to convert only two channels and any of the CCR bytes of the six nonactive channels are in the calibration mode, CA will NOT go active. The user can monitor the CA output to determine when all active channels have completed calibration.

MODE. Mode. This input is used to select between Synchronous Self Clocking Mode (high) or the Synchronous External Clocking Mode (low).

$\overline{RSTI/O}$. Reset I/O. This active low asynchronous input is used to reset the serial interface state machine. This reset only affects the I/O logic and does not affect the Control Register, Channel Configuration Register or Calibration RAMs. This effectively aborts any communication cycle and places the device in a standby mode awaiting the next IR cycle.

Serial Interface Communication

It is useful to think of the HI7188 interface in terms of communication cycles. Each communication cycle happens in 2 phases. The first phase is the writing of an instruction byte while the second phase is the data transfer as described by the instruction byte. It is important to note that phase 2 of the communication cycle can be a single byte or a multi-byte transfer of data including a Burst RAM read/write. It is up to the user to maintain synchronism with respect to data transfers. If the system processor “gets lost”, during an I/O operation, the only way to recover is to reset the Serial Interface via a $\overline{RSTI/O}$. Figure 15 shows both a 2-wire and a 3-wire data transfer.

Instruction Byte Phase

The instruction byte phase initiates a data transfer sequence. The processor writes an eight bit byte to the “Instruction Register”, known as the “Instruction Byte”. The instruction byte informs the HI7188 about the Data cycle phase activities and includes the following information:

- Read or Write Cycle
- Number of Bytes to be Transferred
- Which Register and Starting Byte to be Accessed

Data Cycle Phase

In the data cycle phase, data transfer takes place as defined by the Instruction Register Byte. See Write Operation and Read Operation sections for detailed descriptions. It is important to note that phase 2 of the communication cycle can be a multi-byte transfer of data.

For example, the 4 byte Channel Configuration register can be read using one multi-byte communication cycle rather than four single byte communication cycles. After phase 2 is completed the HI7188 I/O logic enters a standby mode while waiting to receive a new instruction byte. It is up to the user to maintain synchronism with respect to data transfers. If the system processor “gets lost” the only way to recover is to reset the HI7188.

Serial Interface Format

Several formats are available for reading from and writing to the HI7188 registers in both the 2-wire and 3-wire protocols.

Please refer to Figure 15. A portion of these formats is controlled by the CR<2:1> (BD and $\overline{MSB}$) bits which control the byte direction and bit order of a data transfer respectively. These two bits can be written in any combination but only the two most useful will be discussed here. The first combination is to reset both the BD and $\overline{MSB}$ bits (BD = 0, $\overline{MSB}$ = 0). This sets up the interface for descending byte order and MSB first format. When this combination is used the user should always write the instruction register such that the starting byte is the most significant byte address. For example, read three bytes of data starting with the most significant byte. The first byte read will be the most significant in MSB to LSB format. The next byte will be the next least significant (recall descending byte order) again in MSB to LSB order. The last byte will be the next lesser significant byte in MSB to LSB order. THE ENTIRE WORD WAS READ MSB TO LSB format. The second combination is to set both the BD and $\overline{MSB}$ bits to 1. This sets up the interface for ascending byte order and LSB first format. When this combination is used the user should always write the instruction register such that the starting byte is the least significant byte address. For example, read three bytes of data starting with the least significant byte. The first byte read will be the least significant in LSB to MSB format. The next byte will be the next greater significant (recall ascending byte order) again in LSB to MSB order. The last byte will be the next greater significant byte in LSB to MSB order. THE ENTIRE WORD WAS READ LSB TO MSB format. After completion of each communication cycle, The HI7188 interface enters a standby mode while waiting to receive a new instruction byte.

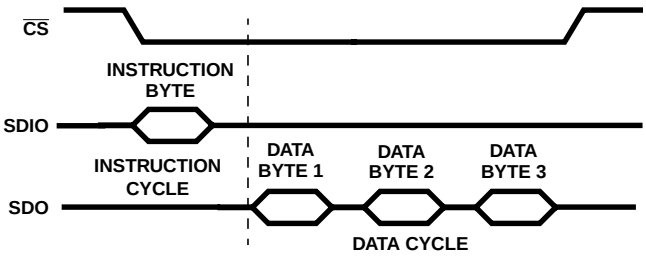


FIGURE 15. 3-WIRE, 3 BYTE READ TRANSFER

Die Characteristics

DIE DIMENSIONS:

215 mils x 257 mils
(5466µm x 6536µm)

METALLIZATION:

Type: AlSiCu
Thickness:Metal 2 16kÅ
Metal 1 6kÅ

SUBSTRATE POTENTIAL:

AV_{SS}

PASSIVATION:

Type: Sandwich
Nitride Thickness: 8kÅ
USG Thickness: 1kÅ

WORST CASE CURRENT DENSITY:

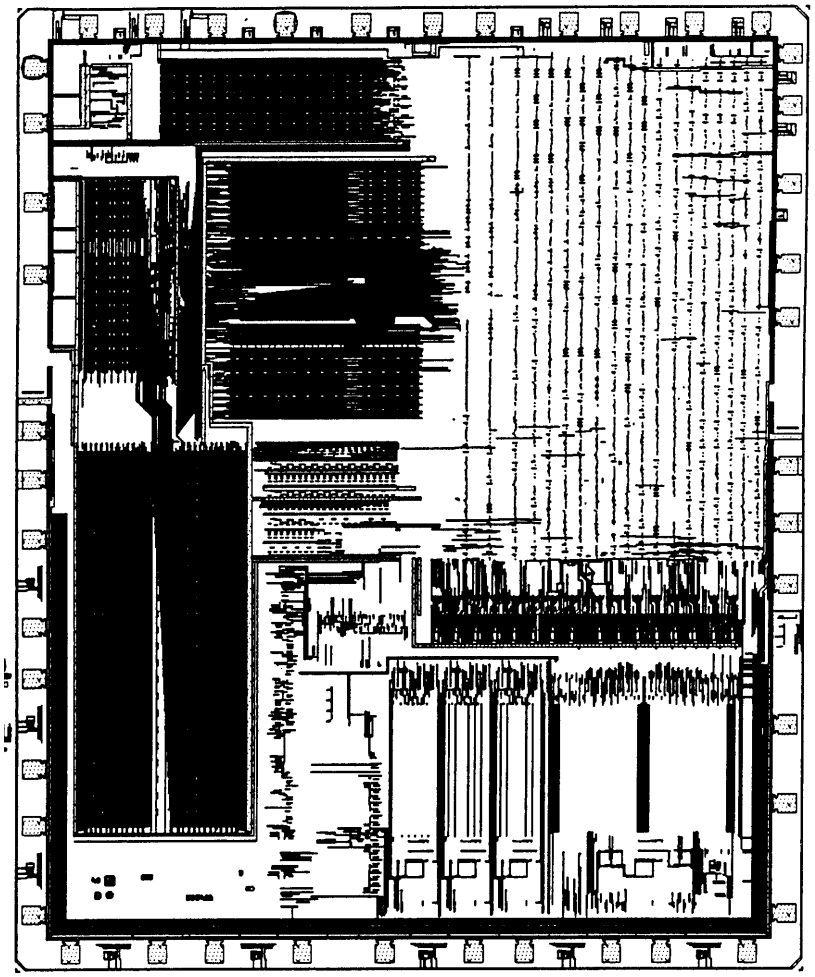
$<2.0 \times 10^5$ A/cm^2

PROCESS:

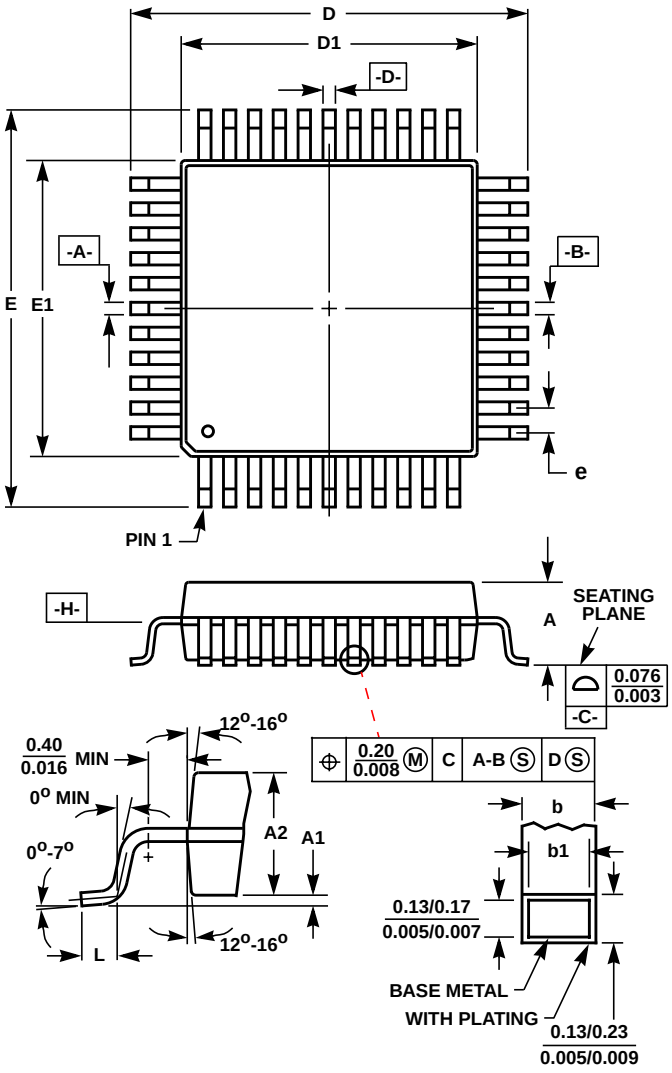
HBCIO

Metallization Mask Layout

HI7188



Metric Plastic Quad Flatpack Packages (MQFP)



Q44.10x10 **(JEDEC MS-022AB ISSUE B)**
44 LEAD METRIC PLASTIC QUAD FLATPACK PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.096	-	2.45	-
A1	0.004	0.010	0.10	0.25	-
A2	0.077	0.083	1.95	2.10	-
b	0.012	0.018	0.30	0.45	6
b1	0.012	0.016	0.30	0.40	-
D	0.515	0.524	13.08	13.32	3
D1	0.389	0.399	9.88	10.12	4, 5
E	0.516	0.523	13.10	13.30	3
E1	0.390	0.398	9.90	10.10	4, 5
L	0.029	0.040	0.73	1.03	-
N	44		44		7
e	0.032 BSC		0.80 BSC		-

Rev. 2 4/99

NOTES:

1. Controlling dimension: MILLIMETER. Converted inch dimensions are not necessarily exact.
2. All dimensions and tolerances per ANSI Y14.5M-1982.
3. Dimensions D and E to be determined at seating plane -C-.
4. Dimensions D1 and E1 to be determined at datum plane -H-.
5. Dimensions D1 and E1 do not include mold protrusion. Allowable protrusion is 0.25mm (0.010 inch) per side.
6. Dimension b does not include dambar protrusion. Allowable dambar protrusion shall be 0.08mm (0.003 inch) total.
7. “N” is the number of terminal positions.

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