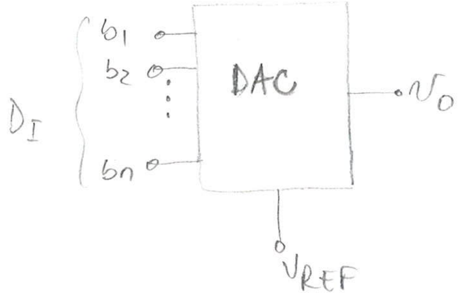
Ch.12 Part 1

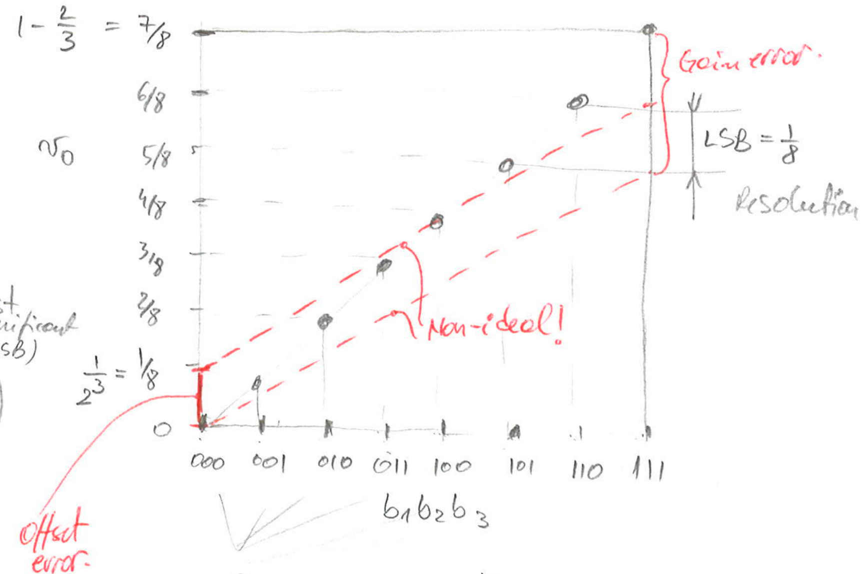
$\boxed{\text{DA and AD converters}}$

Huge topic!

DA converters (DAC)



ideal transfer characteristic



2^n points. → 2^n output values!

Most significant (MSB)

Least significant (LSB)

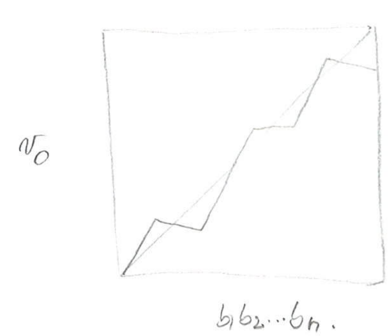
$$v_O = k\cdot V_{REF}\cdot D_I$$
$$= k\cdot V_{REF}\left(b_1\cdot\frac{1}{2}+b_2\cdot\frac{1}{2^2}+\dots b_n\cdot\frac{1}{2^n}\right)$$
$$= k\cdot V_{REF}\sum_{i=1}^{n}\frac{b_i}{2^i}$$

This is called a multiplying DAC because v_O is obtained by multiplying $V_{REF}\times D_I$

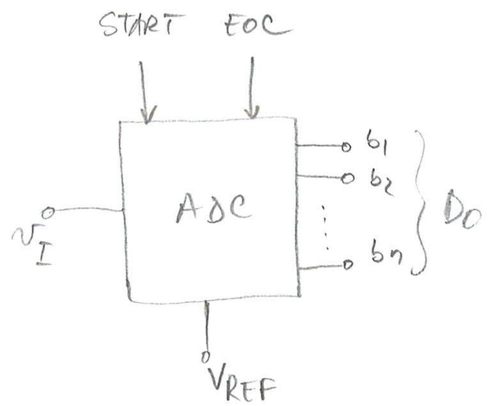
$$D_I = b_1\cdot 2^{-1}+b_2\cdot 2^{-2}+\dots+b_n\cdot 2^{-n}.$$

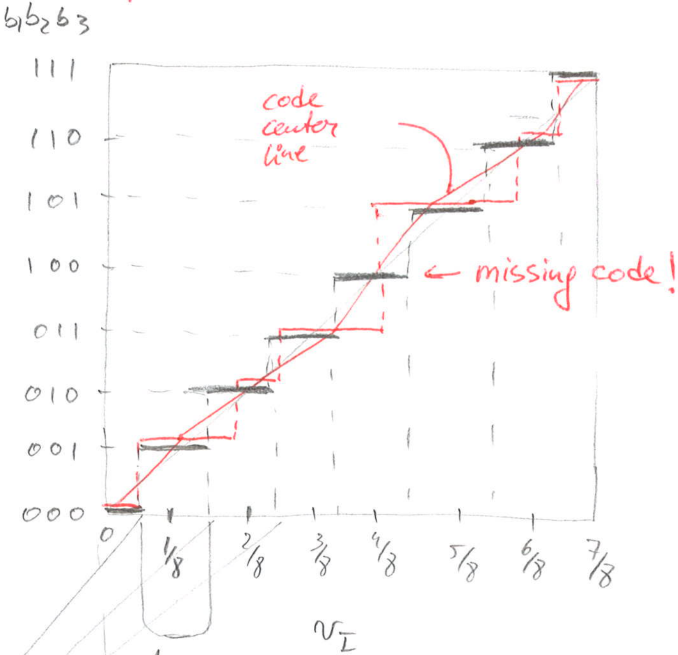
Definitions:
- full scale range (FSR): $\boxed{V_{FSR}=kV_{REF}}$
- full scale value (FSV): $\boxed{V_{FSV}=(1-2^{n})V_{FSR}.}$
- Resolution: LSB is $\boxed{\frac{V_{FSR}}{2^n}}$
- integral nonlinearity
- Differential nonlinearity.

The most important characteristic is $\boxed{\text{monotonicity}}$



AD converters (ADC) - provides the inverse function of a DAC !



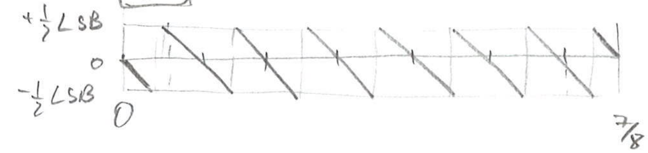


$$D_0 = b_1 \cdot \frac{1}{2} + b_2 \cdot \frac{1}{2^2} + \dots + b_n \cdot \frac{1}{2^n}$$

$$= \frac{v_I}{k \cdot V_{REF}} = \frac{v_I}{V_{FSR}}.$$

Any input value in this range will be coded as 001! We have an error. ≙ quantization error. $\boxed{e_q}$

$\boxed{e_q}$

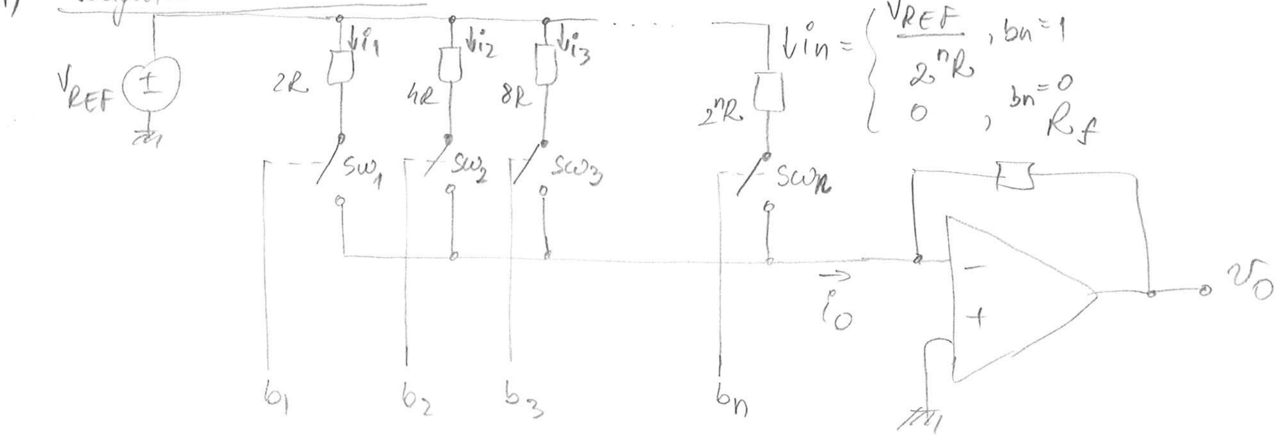


ideally these transitions take place at **odd** number of $\frac{1}{2}$LSB! if not we have nonlinearities/errors.

Conversion time ≙ time for ADC to complete the transition!

Examples

1) Weighted resistor DAC



$$\frac{v_O}{R_f} = -i_o$$

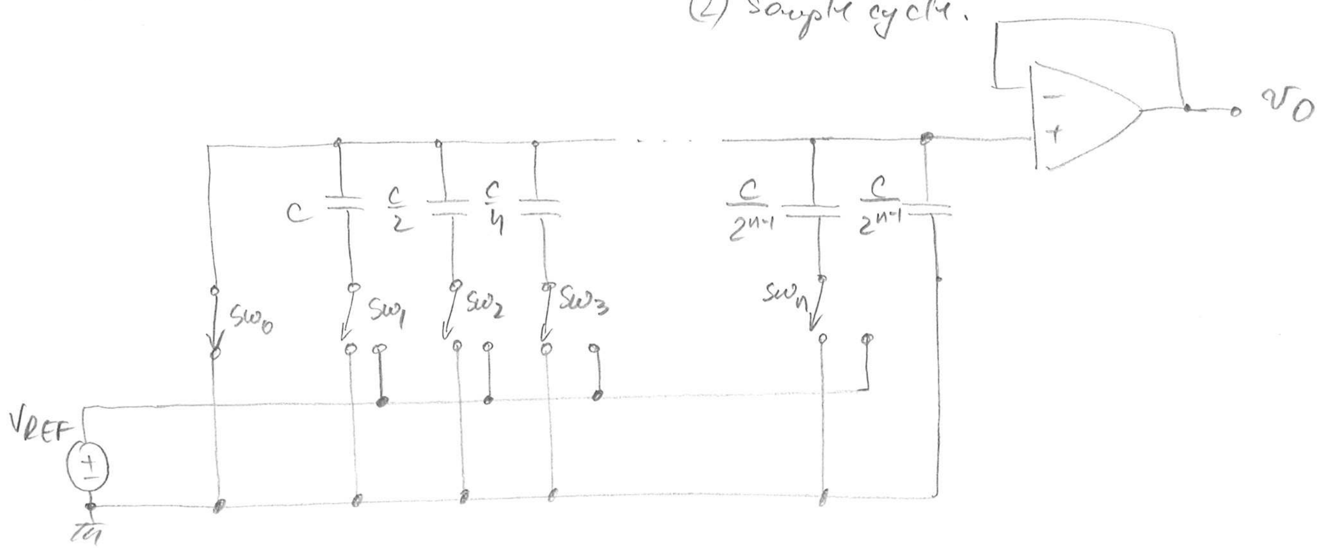
$$v_O = -\frac{R_f}{R} \cdot V_{REF} \cdot \left(b_1 \cdot \frac{1}{2} + b_2 \cdot \frac{1}{4} + b_3 \frac{1}{2^3} + \dots + b_n \frac{1}{2^n}\right)$$

Drawbacks: - nonzero switch resistances!

- a wide spread of resistance values: exponential increase!

2) Weighted-capacitor DAC

Operation alternates between (1) reset cycle: for resetting.
(2) sample cycle.



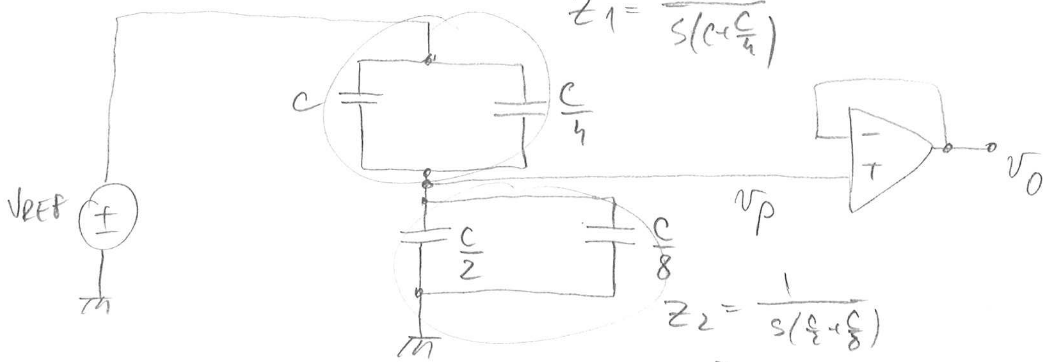
$$v_O = V_{REF} \cdot \frac{C_r}{C_t = 2C}$$

$C_r = \sum$ of capacitances connected to V_{REF}

$C_t = \sum$ of all capacitors!

$$v_O = V_{REF}\left(b_1 2^{-1} + b_2 2^{-2} + \dots + b_n 2^{-n}\right)$$

Detail:



$$Z_1 = \frac{1}{s(C+\frac{C}{4})}$$

$$Z_2 = \frac{1}{s(\frac{C}{2}+\frac{C}{8})}$$

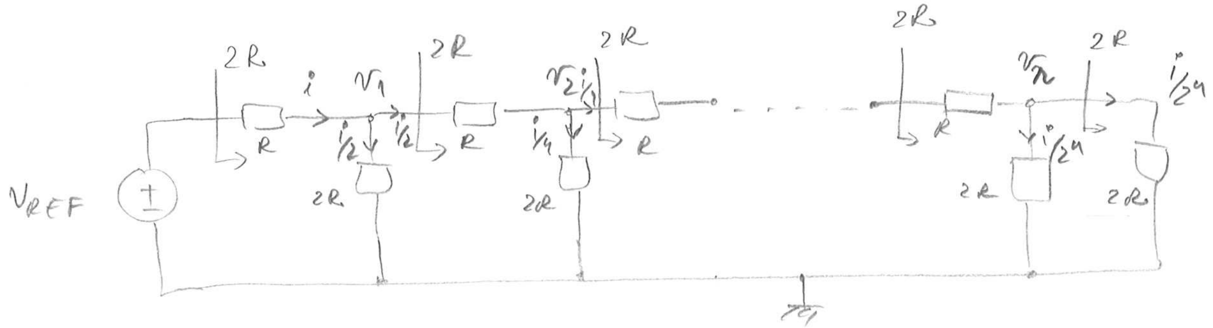
$$v_p = \frac{Z_2}{Z_1+Z_2}\cdot V_{REF} = \frac{\frac{1}{s(\frac{C}{2}+\frac{C}{8})}}{\frac{1}{s(\frac{C}{2}+\frac{C}{8})}+\frac{1}{s(C+\frac{C}{4})}} = \frac{\frac{1}{(\frac{C}{2}+\frac{C}{8})}}{\frac{C+\frac{C}{2}+\frac{C}{4}+\frac{C}{8}}{(\frac{C}{2}+\frac{C}{8})(C+\frac{C}{4})}} = \frac{\overbrace{C+\frac{C}{4}}^{C_r}}{C_t} = \frac{C_r}{C_t}$$

Advantage: + MOS capacitors can be controlled to 0.1% accuracies

Disadvantage: − exponentially increasing values for capacitors!

3) Potentiometric DAC's

4) $\boxed{\text{R-2R ladders}}$: used by most popular DAC!

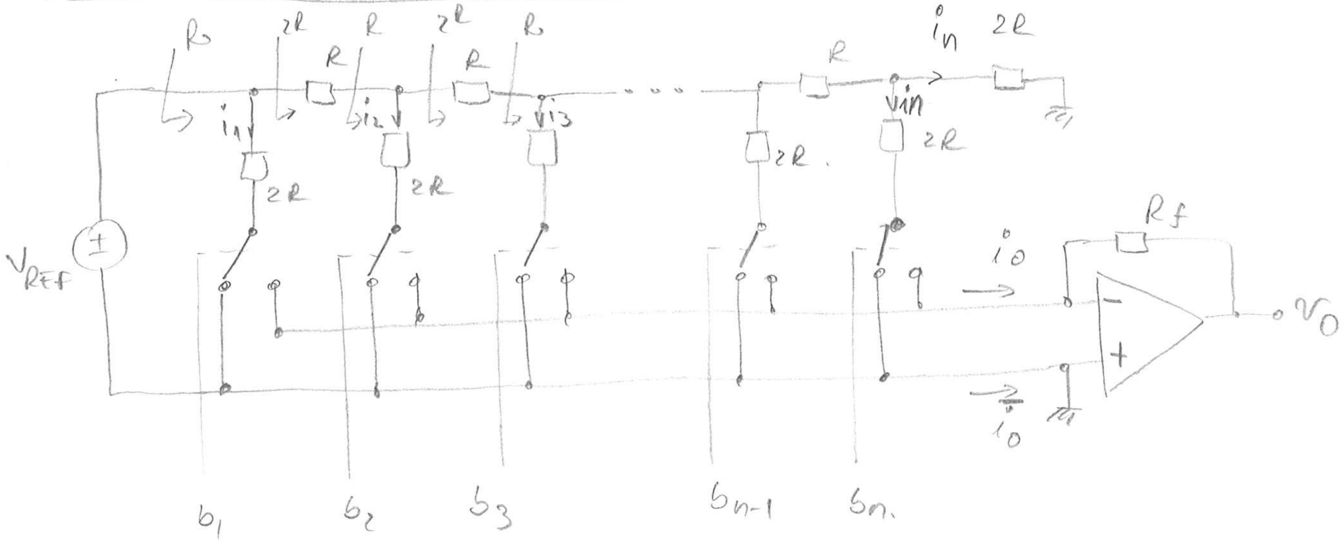


$$i_{k+1} = \frac{1}{2} i_k \quad , \quad v_{k+1} = \frac{1}{2} v_k$$

⊕ Can be fabricated monolithically, on chip.

⊕ just two resistance values!

5) Current-mode R-2R ladder



$$\begin{cases} i_1 = \dfrac{V_{REF}}{2R} = \dfrac{V_{REF}}{R} \cdot \dfrac{1}{2} \\ i_2 = \dfrac{V_{REF}}{4R} = \dfrac{V_{REF}}{R} \cdot \dfrac{1}{2^2} \\ \ldots \\ i_n = \dfrac{V_{REF}}{R} \cdot \dfrac{1}{2^n} \end{cases}$$

$$\frac{v_O}{R_f} = -i_o$$

$$v_O = -R_f \cdot i_o$$

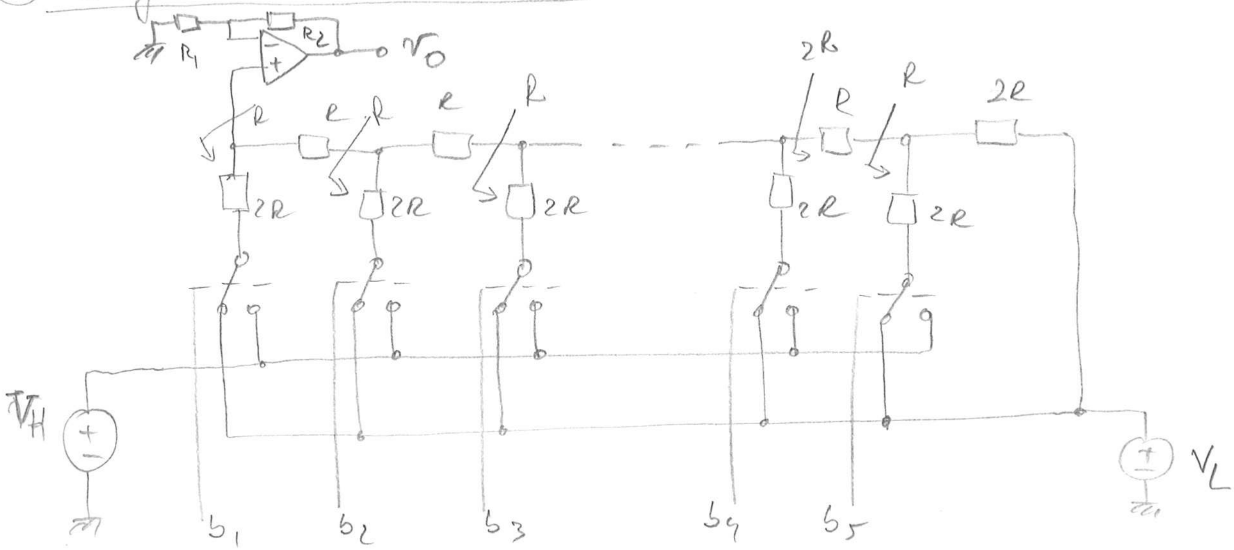
$$v_O = -\frac{R_f}{R} V_{REF} \left(b_1 \cdot \frac{1}{2} + b_2 \cdot \frac{1}{2^2} + \ldots + b_n \cdot \frac{1}{2^n} \right)$$

$$\triangleq K = -\frac{R_f}{R}$$

Note that $i_o + \bar{i}_o = (1 - 2^{-n}) \dfrac{V_{REF}}{R}$ regardless of $D_I = b_1 b_2 \ldots b_n$!

$\bar{i}_o \triangleq$ is said to be complementary to i_o.

(6) Voltage-mode R-2R ladder



$$LSB = \frac{V_H - V_L}{2^n}$$

from

$$V_L \div \left(1 - \frac{1}{2^n}\right)(V_H - V_L)$$

$$K = 1 + \frac{R_2}{R_1}$$

Advantage: we can interpolate between any V_L, V_H

Segmentation

High resolution DAC are obtained (for $n>12$) using a hybrid approach.

<u>The idea:</u>

Master $LSB_M = \frac{1}{2^4}(V_H - V_L)$ 16 segments in this case!

V_L segment $V_L + LSB_M$ segment $V_L + 2LSB_M$ segment $V_H - LSB_M$ segment V_H

16 bit DAC

1) Divide it into 16 equal segments, sum of segments acts as bias.
2) Every segment, then is interpolated by the same 12 bit DAC.

$\underbrace{b_1 b_2 b_3 b_4}_{\text{control the segments}} \; \underbrace{b_5 b_6 \dots b_{16}}_{\text{form a 12 bit DAC for each segment}}$

control the segments used as inputs to a decoder typically.

form a 12 bit DAC for each segment

⊕ In this way monotonicity is easier to achieve!