Ch. 5 Static Op Amp Limitations

Idea: study one limitation at a time, assuming that the Op Amp is otherwise ideal.

- input bias current I_B
- input offset current I_{OS}
- input offset voltage V_{OS}
- thermal drift $TC(V_{OS})$
- CMRR, PSRR
- gain nonlinearity.

5.2 Input bias (I_B) and offset (I_{OS}) currents

(I_{offset})

(3) I_P, I_N input Opamp currents.

- base current for biasing Q_1 Q_2 in forward active region.
- they are mismatched due to mismatches in the two halves.

Definitions:

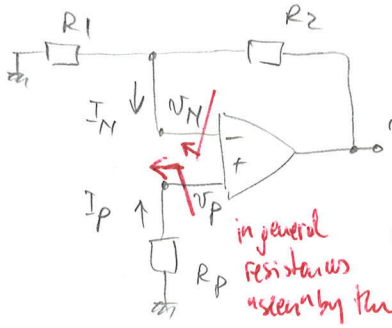
$$\begin{cases} I_B \triangleq \dfrac{I_P + I_N}{2} >> I_{OS} \\ I_{OS} \triangleq I_P - I_N \to 0 \end{cases}$$

Typical values:

$$\begin{cases} I_B = 80\,nA \div 500\,nA \\ I_{OS} = 20\,nA \div 200\,nA \end{cases}$$

Errors caused by I_B, I_{OS}: use two representative cases:

(a)



$$v_O = \left(1 + \frac{R_2}{R_1}\right) v_P + R_2 \cdot I_N$$

in general resistances viewed by the two inputs should be made more or less equal!

$$v_O = R_2 I_N - \left(1 + \frac{R_2}{R_1}\right) \cdot R_P \cdot I_P \triangleq E_O$$

$$\boxed{E_O = \left(1 + \frac{R_2}{R_1}\right)\left[(R_1 \| R_2) I_N - R_P \cdot I_P\right]} \triangleq \text{output error.}$$

- In the absence of any input signal $\Rightarrow$ we have E_O at output. This E_O is unwanted $\triangleq$ **output dc noise.** To get rid of it:

(1) Method 1:

$$\boxed{E_O = \left(1 + \frac{R_2}{R_1}\right)\left\{\left[(R_1 \| R_2) - R_P\right] \cdot I_B - \left[(R_1 \| R_2) + R_P\right] \cdot \frac{I_{OS}}{2}\right\}}$$

Minimized/eliminated by taking $R_P = R_1 \| R_2$!

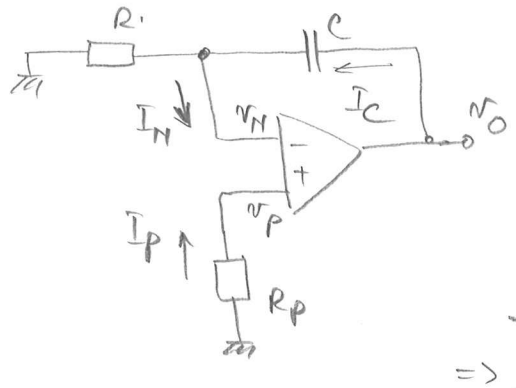
much smaller anyway!

and/or

(2) Method 2: scale down resistances. (power consumption will increase)

$\Rightarrow R_1 \| R_2$ decreases also!

(6)



$$v_N = v_P = -R_P \cdot I_P$$

KCL:

$$I_C = \frac{v_N}{R} + I_N = \frac{1}{R}\left(R I_N - R_P I_P\right) \Rightarrow$$

$$\Rightarrow \boxed{I_C = \frac{1}{R}\cdot\left[(R-R_P)I_B - (R+R_P)\frac{I_{OS}}{2}\right]}$$

$$\Rightarrow v_O(t) = E_O(t) + v_O(0)$$

↑ value of v_O at $t=0$ (initial condition/value)

$$\boxed{E_O(t) = \frac{1}{RC}\int_0^t \left[(R-R_P)I_B - (R+R_P)\frac{I_{OS}}{2}\right] d\tau}$$

$\triangleq$ output error unwanted!

$\triangleq$ input error is integrated over time and out will be saturating to V_{sat+} or V_{sat-} because I_B, I_{OS} are relatively constant.

It's a ramp voltage.

Get rid of $E_O(t)$: (1) install dummy resistance $\boxed{R_P = R}$!

(2) component scaling also.

5.3 Low input-bias current (I_B) Op Amps

Exercize! Techniques to keep I_B, I_{OS} as small as possible.

Note: disadvantage of JFET and MOSFET Op Amps is that I_B varies with temperature, even though it's small (Fig. 5.9).

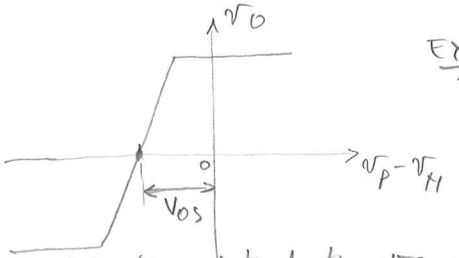
5.4 Input offset voltage V_{OS}

V_{offset} → can be $\mu V \div mV$ range!!!

- if you short inputs of the Op Amp → output ≠ zero!
- due to inherent mismatches of the input-stage ⇒ $v_O \neq 0$ for zero input ≡ i.e. inputs shorted together.

$$v_O = a(v_P - v_N) \neq 0$$

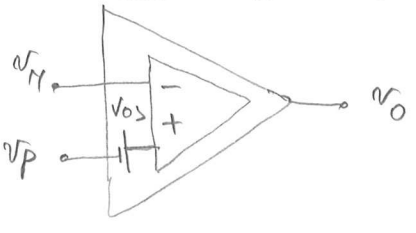
- To force v_O to zero a correcting voltage will have to be applied at the input. This amount is the V_{OS}, the **Input offset voltage**.



Effect of V_{OS} is that the VTC characteristic is shifted!

Example:

μA 741C $V_{OS} = 2mV$

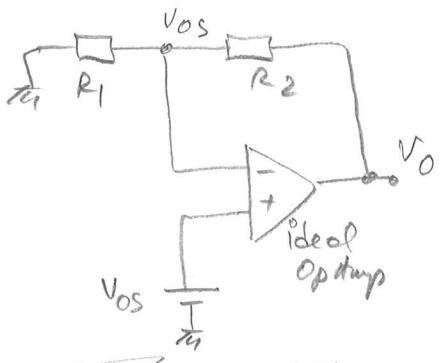


Model for Op Amp

Now VTC is $v_O = a[v_P + V_{OS} - v_N]$ (1)

Errors caused by V_{OS}

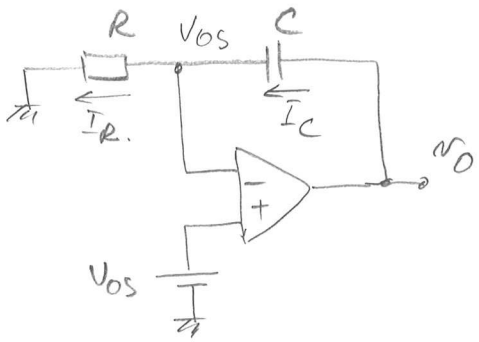
(a)



$$V_O = E_O = \left(1 + \frac{R_2}{R_1}\right) V_{OS}$$

← Output Errors

(b)



$$I_C = I_R = \frac{V_{OS}}{R}$$

$$V_O(t) = E_O(t) + V_O(0)$$

$$E_O(t) = \frac{1}{RC}\int_0^t V_{OS}\, dt$$

Important: V_{OS} is dependent on a couple of factors:

- **Thermal Drift**: V_{OS} is temperature dependent.

  Temperature coefficient $TC(V_{OS}) \triangleq \frac{\partial V_{OS}}{\partial T}$ $\left[\frac{\mu V}{^\circ C}\right]$ (2) ($5\,\mu V/^\circ C$ typically)

Effects that can be modeled/captured by V_{OS}:

- **CMRR**

  Practical opamps are sensitive to common-mode input voltages.

$$V_{CM} = \frac{V_P + V_N}{2}$$

Transfer characteristic in this case is:

$$V_O = a(V_P - V_N) + a_{CM} \cdot V_{CM}$$

$$= a\left[(V_P - V_N) + \frac{a_{CM}}{a} \cdot V_{CM}\right] = a\left[(V_P - V_N) + \frac{V_{CM}}{CMRR}\right] \quad (3)$$

$\frac{a_{CM}}{a} \triangleq \frac{1}{CMRR}$ Definition 1 — compare to (1)

Great idea: "Sensitivity of V_O to V_{CM} could be modeled with an input-offset voltage term of value $\frac{V_{CM}}{CMRR}$!" **Nice!**

=> Second definition of CMRR: $\frac{1}{CMRR} \triangleq \frac{\partial V_{OS}}{\partial V_{CM}}$ (Definition 2) with the interpretation of "change in V_{OS} brought by a change in V_{CM}".

• PSRR

- if we change the supply voltage V_S by the amount ΔV_S
  => operating points of internal devices will change! =>
  => small change in v_O.

Great idea: model this phenomenon with a change in V_{OS}:

$$\frac{1}{PSRR} \triangleq \frac{\partial V_{OS}}{\partial V_S} \qquad \left[\frac{\mu V}{V}\right]$$

• Change of V_{OS} with the Output Swing

- Output swing Δv_O => input will swing with $\frac{\Delta v_O}{a}$
- This effect can be regarded as an effective offset-voltage change.

$$\frac{\Delta v_O}{a} = \Delta V_{OS}$$

Finally: write V_{OS} in terms of various operating changes that affect it:

$$V_{OS} = V_{OS\phi} + TC(V_{OS})\cdot\Delta T + \frac{\Delta v_{CM}}{CMRR} + \frac{\Delta V_S}{PSRR} + \frac{\Delta v_O}{a}$$

- $V_{OS\phi}$: initial input-offset voltage due to mismatches
- $TC(V_{OS})\cdot\Delta T$: because V_{OS} varies with T. All BJT's characteristics vary with T.
- $\frac{\Delta v_{CM}}{CMRR}$: models the variation of v_O as a consequence of the change in v_{CM} (that changes/alters the mismatches)
- $\frac{\Delta V_S}{PSRR}$: same as $\frac{\Delta v_{CM}}{CMRR}$
- $\frac{\Delta v_O}{a}$: Regarding any $v_P - v_N$ change due to v_O change as V_{OS} - because a is finite

Example 5.6

$a = 10^5\ V/V$, $a_{min} = 10^4\ V/V$

$TC(V_{OS})_{avg} = 3\mu V/°C$, $CMRR = PSRR \begin{cases} = 100\,dB & \text{typical} \\ = 80\,dB & \text{min.} \end{cases}$

(?) Worst-case and most probable change of V_{OS} over the following operating ranges: $0°C \le T \le 70°C$

$V_S = \pm 15V \pm 5\%$, $-1 \le V_P \le 1V$, $-5V \le v_O \le 5V$.

$\Delta V_{OS1} = 3\mu V/°C \cdot (70-25)°C = 135\mu V$

$\frac{1}{CMRR} = \frac{1}{PSRR} = \begin{cases} 10^{-100/20} = 10\mu V/V & \text{typical} \\ 10^{-80/20} = 100\mu V/V & \text{max.} \end{cases}$ =>

=> $\Delta V_{OS2} = \pm 1V/CMRR = \pm 10\mu V$, $\pm 100\mu V$ max

(because $v_{CM} \cong v_P$) $\Delta V_{OS3} = 2\times(\pm 0.75V)/PSRR = \pm 15\mu V$, $\pm 150\mu V$ max.

$\Delta V_{OS4} = \pm 5V/a = \pm 5\mu V$, $\pm 500\mu V$ max

=>

① Worst-case V_{OS} change:

$\Delta V_{OS} = \pm(135+100+150+500) = \pm 885\mu V$

② Most probable:

$\Delta V_{OS} = \pm\left(135^2+10^2+15^2+50^2\right)^{\frac{1}{2}} = \pm 145\mu V$

5.5 Low input-voltage (V_{OS}) Op Amps

Exercise!

5.6 Input Offset-error Compensation

The effect of I_{OS} and V_{OS} acting simultaneously:

(a) Inverting/noninverting amplifiers

$$V_O = A_S \cdot V_I + E_O$$

$\triangleq \frac{1}{\beta} \triangleq$ dc noise gain — V_O important!

$$E_O = \left(1 + \frac{R_2}{R_1}\right)\left[V_{OS} - (R_1 \| R_2)\, I_{OS}\right]$$

Total error offset referred @ output.

Signal gain $\triangleq A_S = \begin{cases} -R_2/R_1, & \text{inverting} \\ 1 + \frac{R_2}{R_1}, & \text{non-inverting.} \end{cases}$

$$E_I = V_{OS} - (R_1 \| R_2)\, I_{OS}$$

total error offset referred @ input

(b) Integrator

$$V_O(t) = -\frac{1}{RC}\int_0^t \left[V_I(\tau) + E_I\right] d\tau + V_O(0)$$

$$E_I = R I_{OS} - V_{OS}$$

Can be **Nulled** using { – a trimmer (not advised) — Internal Nulling / External Nulling
– a combination of circuit tricks (resist. scaling and Op Amp Selection).

introduces additional imbalance in CMRR, PSRR

5.7 Maximum Ratings

Exercise!