Project ideas for extra credit
ECE-470 Digital Design II

These are ideas for additional optional projects. You may want to implement any of them. If successfully done you may get up to 5% of the final grade (for each of them). You should talk to the instructor before starting to work on any of these projects.

Project 1

The objective of this project is to implement and simulate in LTSpice an A/D current monitor used to translate the gate current through a DUT (I_G) into a 16 bit digital number. This monitor is part of a test circuit utilized for gate dielectric breakdown characterization. This circuit is discussed in this paper:

- J. Keane, S. Venkatraman, P.F. Butzen, and C.H. Kim, "An array-based test circuit for fully automated gate dielectric breakdown characterization," *IEEE Trans. on Very Large Scale Integration (VLSI) Systems*, pp. 787-795, 2011.

Project 2

The objective of this project is to implement BIST or SCAN design for part(s) of a processor. You will be given the VHDL code of a simple RISC processor (SPIM model). You will have to read and understand its documentation and code. Then, you will have to modify it to add BIST or SCAN to improve its testability. You need to submit a short description of the code, waveforms of its simulation with and without your testability additions.