ECE-470/670 Digital Design II: Syllabus

Fall 2011

Course info
ECE-470/670 Digital Design II, 3 credits
Prereq: ECE-375 with a grade of C or better. Knowledge of C++ and VHDL/Verilog.
Lecture: TuTh 2:00-3:15pm in ECE-243
Course website: http://venus.ece.ndsu.nodak.edu/~cris/ece470/index.html

Instructor
Cristinel Ababei, cristinel.ababei(at)ndsu.edu
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Office hours: Tuesday 10:30-11:30am, Thursday 1:00-2:00pm or by appointment

Bulletin description
Design and analysis of reliable digital systems through robust information coding, fault avoidance, and fault tolerance.

Textbook
[BA05] M. Bushnell and V. Agrawal, *Essentials of Electronic Testing for Digital Memory and Mixed-Signal VLSI Circuits*, Springer 2000. **(required)**.
Recommended:
[ABF94] Miron Abramovici, Melvin A. Breuer, and Arthur D. Friedman, *Digital Systems Testing and Testable Design*, Wiley-IEEE Press, Revised edition, 1994.
[WWW06] Laung-Terng Wang, Cheng-Wen Wu, and Xiaoqing Wen, *VLSI Test Principles and Architectures - Design for Testability*, Elsevier, 2006.
[R07] Charles H. Roth Jr., *Digital Systems Design Using VHDL*, Wadsworth, 2007.

Course objectives
This course examines in depth theories and techniques for testing multimillion transistor VLSI chips. The overall course objective is to teach electrical and computer engineering students the fundamental concepts of testing and reliability, methods of modeling and analysis of faults, and design for testability of digital circuits and systems. Specific objectives include the following:

1. Investigate failure mechanisms and reliability issues of VLSI circuits, and characterize failures at various levels of circuit hierarchy.
2. Utilize logic and fault simulation to develop test vector generation algorithms for combinational and sequential circuits.
3. Develop testing methodologies for memory chips.
4. Coordinate different testing tasks (combinational testing, sequential testing, memory testing, BIST, scan testing, etc.) so that a chip is tested as a whole entity.
5. Utilize data structures and theoretical knowledge about algorithms in C++ programs that are used to implement testing software tools.
6. Utilize VHDL/Verilog to specify digital circuit structure and behavior and Altera FPGA development boards for testing.
7. Conduct literature survey on specific research topics, identify current challenges, and develop solutions.
8. Prepare informative and organized project reports and presentations that describe the methodologies employed, the results obtained, and the conclusions made in simulation experiments.

Relationship of course objectives to ABET Criterion 3 student outcomes (see http://www.abet.org/Linked%20Documents-UPDATE/Program%20Docs/abet-eac-criteria-2011-2012.pdf)

	ABET Criterion 3 student outcome	Course objective(s)
3A	Apply knowledge of mathematics, science, and engineering	1,2,3,4,5,6
3B	Design and conduct experiments, as well as to analyze and interpret data	6,7
3C	Design a system, component, or process to meet desired needs	6,7
3D	Function on multidisciplinary teams	
3E	Identify, formulate, and solve engineering problems	1,2,3,4,5,6
3F	Understanding of professional and ethical responsibility	
3G	Communicate effectively	8
3H	Broad education necessary to understand the impact of engineering solutions	5
3I	Recognition of the need for, and an ability to engage in life-long learning	5,6,7
3J	Knowledge of contemporary issues	7
3K	Use the techniques, skills, and modern engineering tools	3,4,5,6
L	Grow in the knowledge of and make professional contributions to at least one specific area of ECE	7

Grading

Grade breakdown: A=[90-100], B=[80-90), C=[70-80), D=[60-70).

-- Final grade components:
- Exam 1: 25%
- Exam 2 (final): 25%
- Homework: 15%
- Projects: 35%

-- Makeup exams will only be allowed in special situations. The extraordinary circumstances requiring a makeup exam must be verifiable.

Homework

-- Homework submissions are due before class starts. No late submissions are accepted.

-- If you are absent from class or you know that you will be absent from class, you should as soon as possible arrange with the instructor for any missed work. It is the student's responsibility to contact the instructor in such a case. Arrangements made in advance of an absence (if approved -- depends on the reason of absence) may allow full credit to be given for late work.

-- Collaboration on homework is ok, copying is not ok; a separate solution is required for each student.

-- Include your name on all homework assignments, reports, and exams.

Projects

Undergraduates will work on two course projects, which will require programming in C++ and VHDL/Verilog. Graduate students will work in addition on a third course project. The third project will require to survey literature to identify a current problem (in testing or reliability), to propose a solution, and to implement it.

Special needs

Any students with disabilities or other special needs, who need special accommodations in this course, are invited to share these concerns or requests with the instructor as soon as possible.

Veterans and soldiers

Veterans and student soldiers with special circumstances or who are activated are encouraged to notify the instructor in advance.

Academic honesty
All work in this course must be completed in a manner consistent with NDSU University Senate Policy, Section 335: Code of Academic Responsibility and Conduct. Violation of this policy will result in receipt of a failing grade. Please read: http://www.ndsu.edu/fileadmin/policy/335.pdf

Others
-- While university regulations do not require attendance in class, the student should know that there may be material covered in class which is not discussed in the text or which may be discussed in a different manner than presented in the text. The student is responsible for all the material discussed in class whether or not the student was in class. If the student misses a class period, it is the student's responsibility to obtain the notes from a classmate.
-- If the student has questions about the way a particular homework or exam problem was graded, s/he should discuss this with the instructor during office hours. However, this must be done within one week the exam or homework was returned to the class. This does not apply to the final exam.
-- Questions during class are highly encouraged.
-- Do not pack your stuff and get ready to leave with minutes before the lecture is over -- this annoys your colleagues.
-- Usage of cell phones, laptops, newspapers, magazines, etc. is not allowed during lectures.

Course outline and schedule (NOTE: This is subject to change during the term.)

Week	Day and date	Chapter	Topics
1	Tu Aug. 23 Th Aug. 25	1	Introduction *Project 1 discussion*
2	Tu Aug. 30 Th Sep. 1	2,3 4	Testing concepts. Test economics Fault modeling
3	Tu Sep. 6 Th Sep. 8	5 6, [ABF94]-6	Logic and fault simulation Testability measures Fault oriented ATG, ATG common concepts, DJ frontiers
4	Tu Sep. 13 Th Sep. 15	7, [ABF94]-6	Combinational circuit test generation. ATG for SSFs: D algorithm ATG for SSFs: PODEM algorithm, Random TG
5	Tu Sep. 20 Th Sep. 22	8, [ABF94]-6	Sequential circuit test generation, Random test generation
6	Tu Sep. 27 Th Sep. 29	9	Memory test
7	Tu Oct. 4 Th Oct. 6	14, [ABF94]-9	Design for testability (DFT), Generic scan design, Partial scan
8	Tu Oct. 11 Th Oct. 13	16, [ABF94]-9.10, 10	Boundary scan, Compression techniques
9	Tu Oct. 18 Th Oct. 20	15, [ABF94]-11.2	Built-in self-test (BIST) Test pattern generation (TPG)
10	Tu Oct. 25 Th Oct. 27	15, [ABF94]-11.3, 11.4	BIST: Response compaction, Generic and specific architectures *Project 1 final report due*
11	**Tu Nov. 1** Th Nov. 3	 15, [ABF94]-11.4, 18	**EXAM 1 (closed book & notes)** BIST: BILBO, Circular self-test, System test *Project 2 discussion*
12	Tu Nov. 8 Th Nov. 10	Assigned articles	Circuit level reliability
13	Tu Nov. 15 Th Nov. 17	Assigned articles	Circuit level reliability
14	Tu Nov. 22 **Th Nov. 24**	Assigned articles	Circuit level reliability *Project 2 final report due; Project 3 discussion* HOLIDAY - Thanksgiving (no classes)

15	Tu Nov. 29 Th Dec. 1	Assigned articles	Architecture level reliability
16	Tu Dec. 8 Th Dec. 9	Assigned articles	Architecture level reliability *Project 3 presentations*
17	**Th Dec 15**		**EXAM 2 final (closed book & notes) 3:15-5:15pm**

Prepared by: Cristinel Ababei
Date: August 19 2011