EECE-4740 "Advanced VHDL and FPGA Design

Timing Analysis – Intel Quartus II

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BE THE DIFFERENCE.

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Timing Analysis
TimeQuest

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TimeQuest and Synopsis Design Constraint (sdc) File

1. TimeQuest Timing Analyzer
   - TimeQuest Timing Analyzer: Native SDC Support for Timing Analysis of FPGA-Based Designs (8 pages; old, but concepts remain the same)
     - https://www.altera.com/content/dam/altera-www/global/en_US/pdfs/literature/wp/wp-tmqst.pdf
   - Intel Quartus Prime Standard Edition User Guide - Timing Analyzer (91 pages)
     - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/ug/ug-qps-timing-analyzer.pdf
2. Synopsis Design Constraint (sdc) File
   - TimeQuest requires information about connections and devices from Synopsis Design Constraint (sdc) file.
     - https://www.vlsi-expert.com/2011/02/synopsys-design-constraints-sdc-basics.html

Scenarios

- Scenario #1: Portion of RTL circuit; combinational circuit stage wrapped by input and output registers, which share the same clock signal. Example: pipeline stage in RISC-V processor design entity.
- Scenario #2: Typical sequential circuit implementation of a Mealy/Moore FSM. Example: edge_detection design entity.
- Scenario #3: Simple combinational circuit. Example: fourbit_adder design entity.

Scenario #1
RTL circuit

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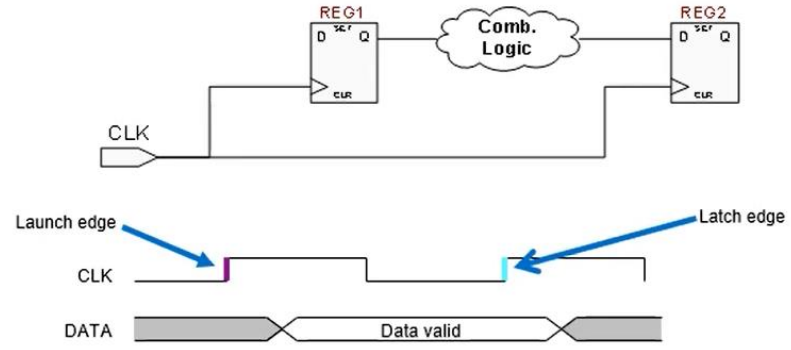
Launch and Latch Edges of Clock Signal



Launch edge:	the edge which "launches" the data from the source register
Latch edge:	the edge which "latches" the data at the destination register (with respect to the launch edge, selected by timing analyzer; typically 1 clock cycle, i.e. rising to rising edge)

Source: https://www.youtube.com/watch?v=HMAqjjCuDEI

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Clock Frequency

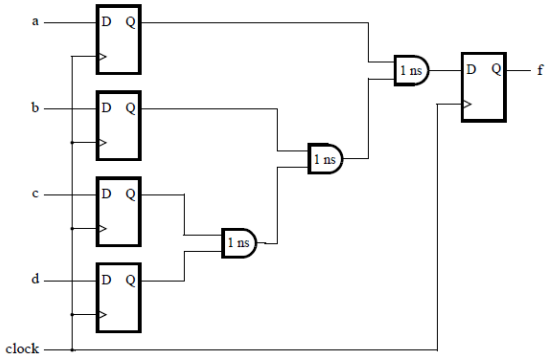

Figure 1. A example for timing analysis.

Maximum clock frequency you can operate this circuit at:

$$f_{max} = \frac{1}{t_{cq} + 3 \times t_{and} + t_{su}} = \frac{1}{5\ \text{ns}} = 200\ \text{MHz}$$

- Using TimeQuest Timing Analyzer (18 pages)
  - http://mems.ece.dal.ca/eced4260/Timequest.pdf

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Design Example

- Using TimeQuest Timing Analyzer (18 pages)
  - http://mems.ece.dal.ca/eced4260/Timequest.pdf
- Create new Quartus Project
  - Provided as example1_quartus/
  - Use target the DE1-SoC Board

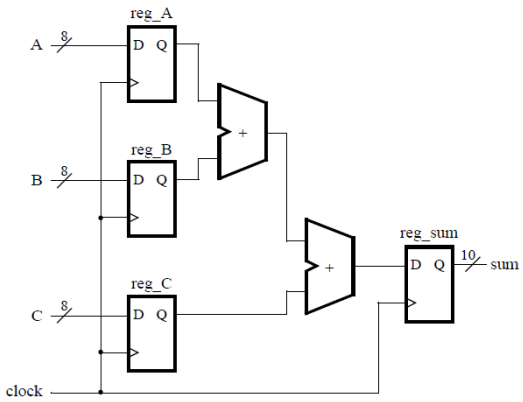

Figure 3. Diagram of the example circuit.

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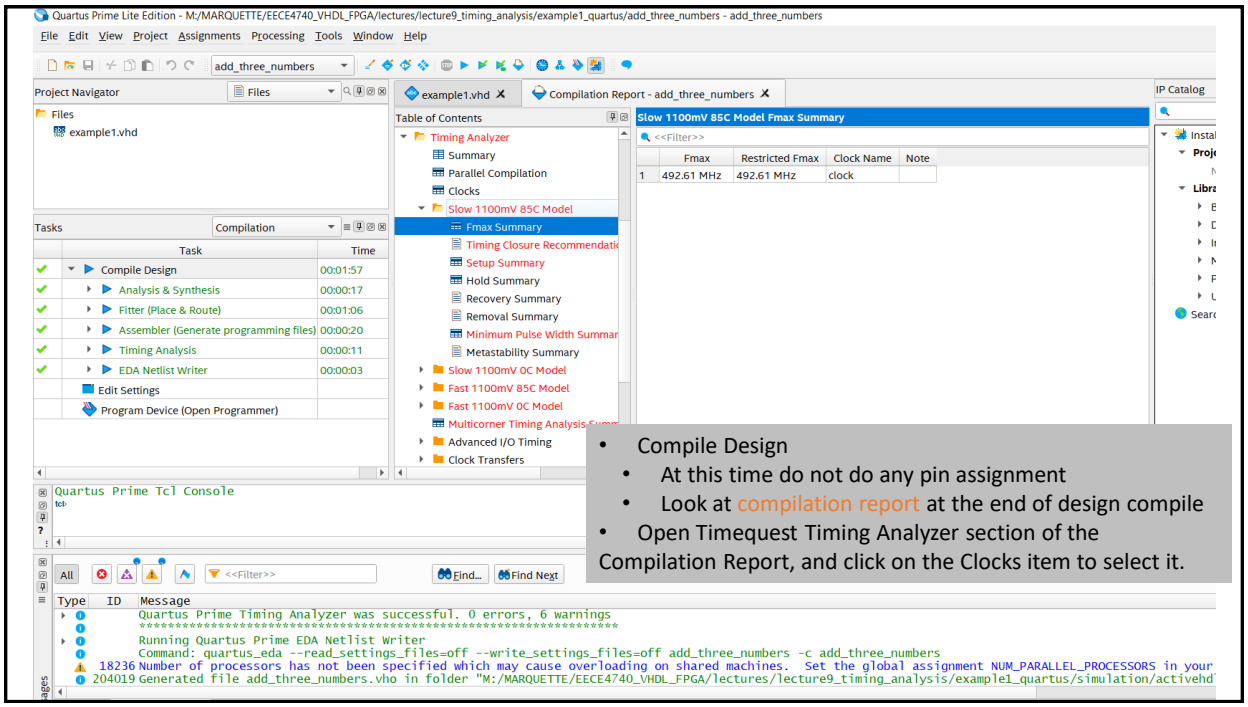

- Compile Design
  - At this time do not do any pin assignment
  - Look at compilation report at the end of design compile
- Open Timequest Timing Analyzer section of the Compilation Report, and click on the Clocks item to select it.

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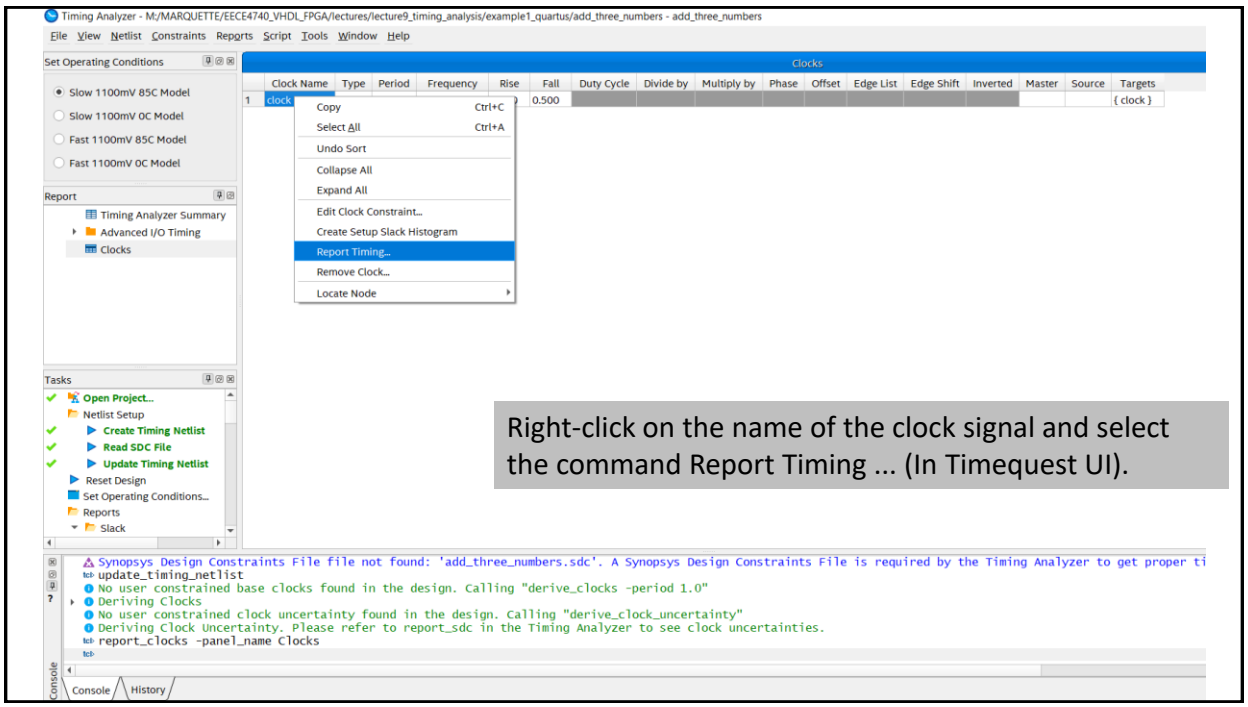

Right-click on the name of the clock signal and select the command Report Timing ... (In Timequest UI).

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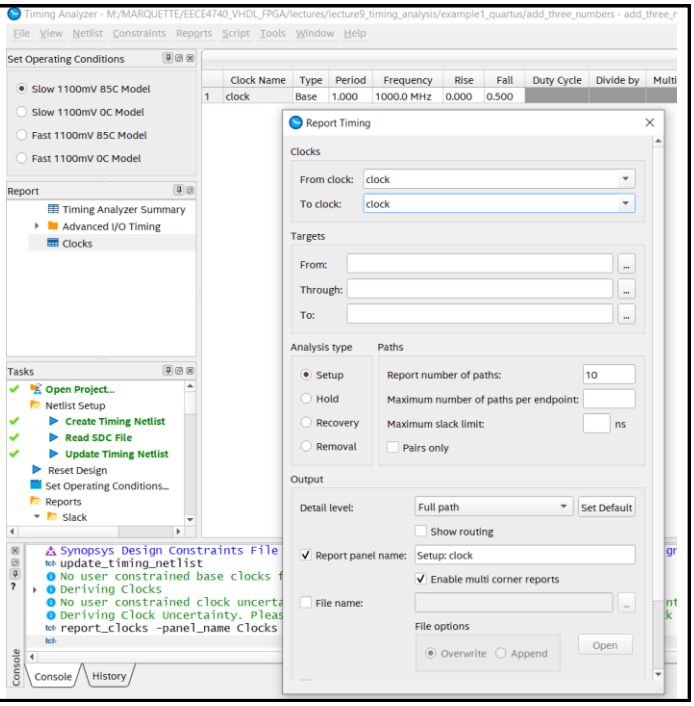
- Click the drop-down arrow in the From clock item and select the clock signal.
- This selection is used to instruct TimeQuest to analyze all paths in the example circuit that start and end at flip-flops that are clocked by the clock signal.
- Accept all of the other default selections and click on the Report Timing button.
- Default clock constraint is 1 ns
- This command opens the Timequest Graphical User Interface (GUI), as depicted in next slide.



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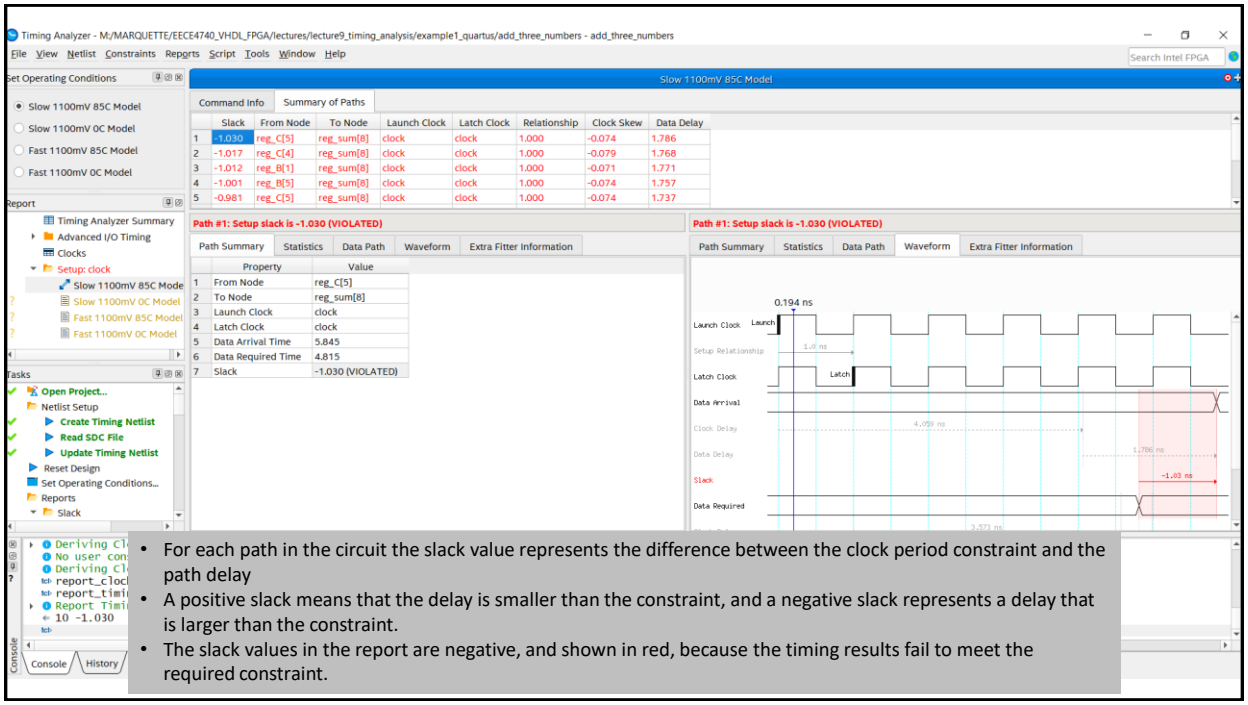

- For each path in the circuit the slack value represents the difference between the clock period constraint and the path delay
- A positive slack means that the delay is smaller than the constraint, and a negative slack represents a delay that is larger than the constraint.
- The slack values in the report are negative, and shown in red, because the timing results fail to meet the required constraint.

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Setting Up Timing Constraints for a Design

- In TimeQuest GUI, select Constraints->Create Clock, which leads to the Create Clock window
- Set the Clock name to clock and the Period to 4.000 ns.
- Click the ... button to the right of the Targets field, leading to the Name Finder window.
- Click List to show all of the ports in the design.
- In the list of ports, highlight clock, which is the clock signal in our circuit, press >, then click OK.
- Finally, click the Run button in the Create Clock window to apply the constraint.
- To use this clock constraint for all future compilations and timing analysis of this project, we must save the constraint to a file of the type sdc which stands for Synopsys* Design Constraint.
- This file uses an industry standard format for specifying timing constraints.
- Select Constraints->Write SDC File... to write all of the currently set constraints (in our case just the one clock constraint) to an SDC file.
- Right-click the report and select Regenerate to re-run the timing analysis using the new 4 ns clock period constraint.
- This analysis results in a positive slack of 1.970 ns.

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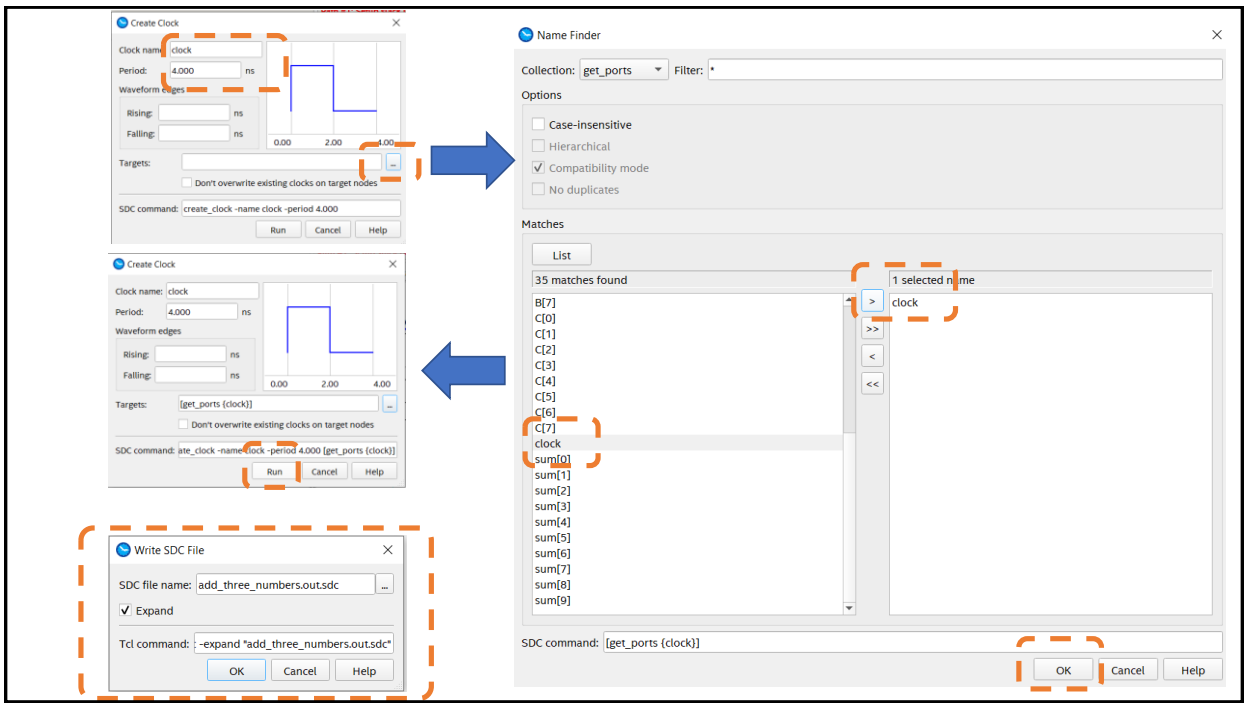

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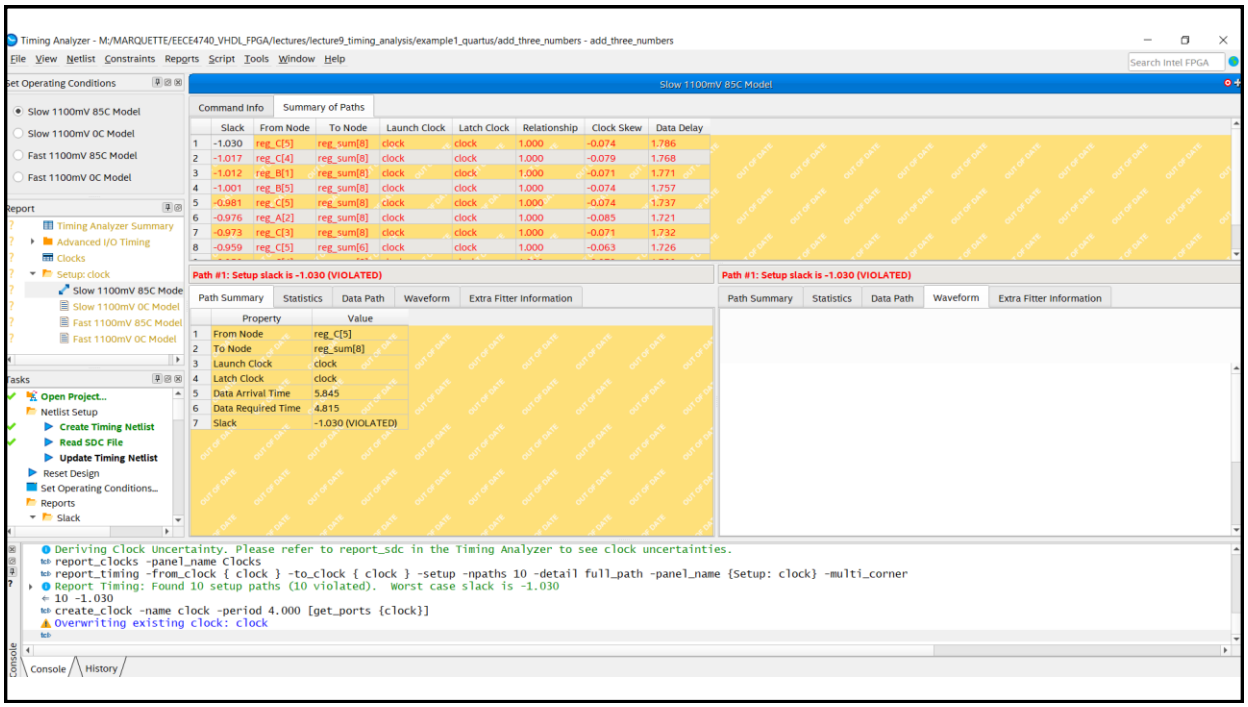
Timing Analyzer - M:/MARQUETTE/EECE4740_VHDL_FPGA/lectures/lecture9_timing_analysis/example1_quartus/add_three_numbers - add_three_numbers
File View Netlist Constraints Reports Script Tools Window Help
Slow 1100mV 85C Model
Command Info
Summary of Paths
Slack From Node To Node Launch Clock Latch Clock Relationship Clock Skew Data Delay
-1.030 reg_C[5] reg_sum[8] clock clock 1.000 -0.074 1.786
-1.017 reg_C[4] reg_sum[8] clock clock 1.000 -0.079 1.768
-1.012 reg_B[1] reg_sum[8] clock clock 1.000 -0.071 1.771
-1.001 reg_B[5] reg_sum[8] clock clock 1.000 -0.074 1.757
-0.981 reg_C[5] reg_sum[8] clock clock 1.000 -0.074 1.737
-0.976 reg_A[2] reg_sum[8] clock clock 1.000 -0.085 1.721
-0.973 reg_C[3] reg_sum[8] clock clock 1.000 -0.071 1.732
-0.959 reg_C[5] reg_sum[6] clock clock 1.000 -0.063 1.726
Path #1: Setup slack is -1.030 (VIOLATED)
Path Summary Statistics Data Path Waveform Extra Fitter Information
Property Value
From Node reg_C[5]
To Node reg_sum[8]
Launch Clock clock
Latch Clock clock
Data Arrival Time 5.845
Data Required Time 4.815
Slack -1.030 (VIOLATED)
Deriving Clock Uncertainty. Please refer to report_sdc in the Timing Analyzer to see clock uncertainties.
report_clocks -panel_name Clocks
report_timing -from_clock { clock } -to_clock { clock } -setup -npaths 10 -detail full_path -panel_name {Setup: clock} -multi_corner
Report Timing: Found 10 setup paths (10 violated). Worst case slack is -1.030
10 -1.030
create_clock -name clock -period 4.000 [get_ports {clock}]
Overwriting existing clock: clock
Console History

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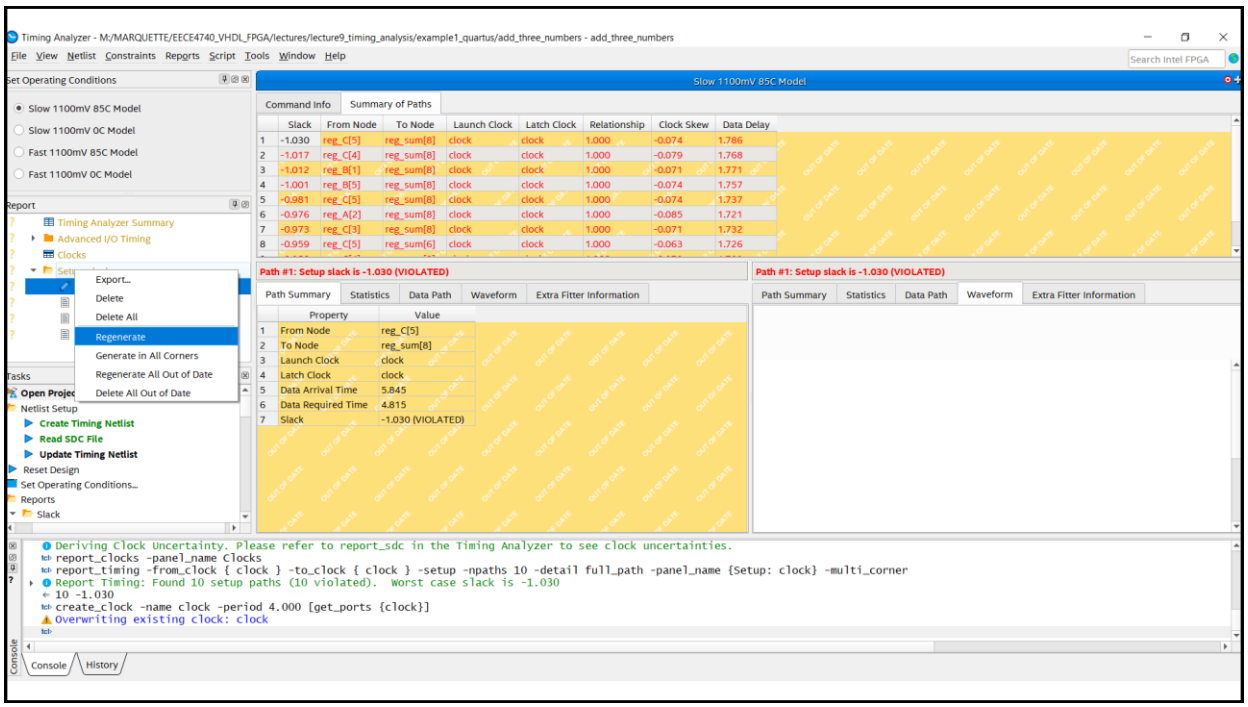
Timing Analyzer - M:/MARQUETTE/EECE4740_VHDL_FPGA/lectures/lecture9_timing_analysis/example1_quartus/add_three_numbers - add_three_numbers
File View Netlist Constraints Reports Script Tools Window Help
Slow 1100mV 85C Model
Export...
Delete
Delete All
Regenerate
Generate in All Corners
Regenerate All Out of Date
Delete All Out of Date
Path #1: Setup slack is -1.030 (VIOLATED)
Deriving Clock Uncertainty. Please refer to report_sdc in the Timing Analyzer to see clock uncertainties.
report_clocks -panel_name Clocks
report_timing -from_clock { clock } -to_clock { clock } -setup -npaths 10 -detail full_path -panel_name {Setup: clock} -multi_corner
Report Timing: Found 10 setup paths (10 violated). Worst case slack is -1.030
10 -1.030
create_clock -name clock -period 4.000 [get_ports {clock}]
Overwriting existing clock: clock
Console History

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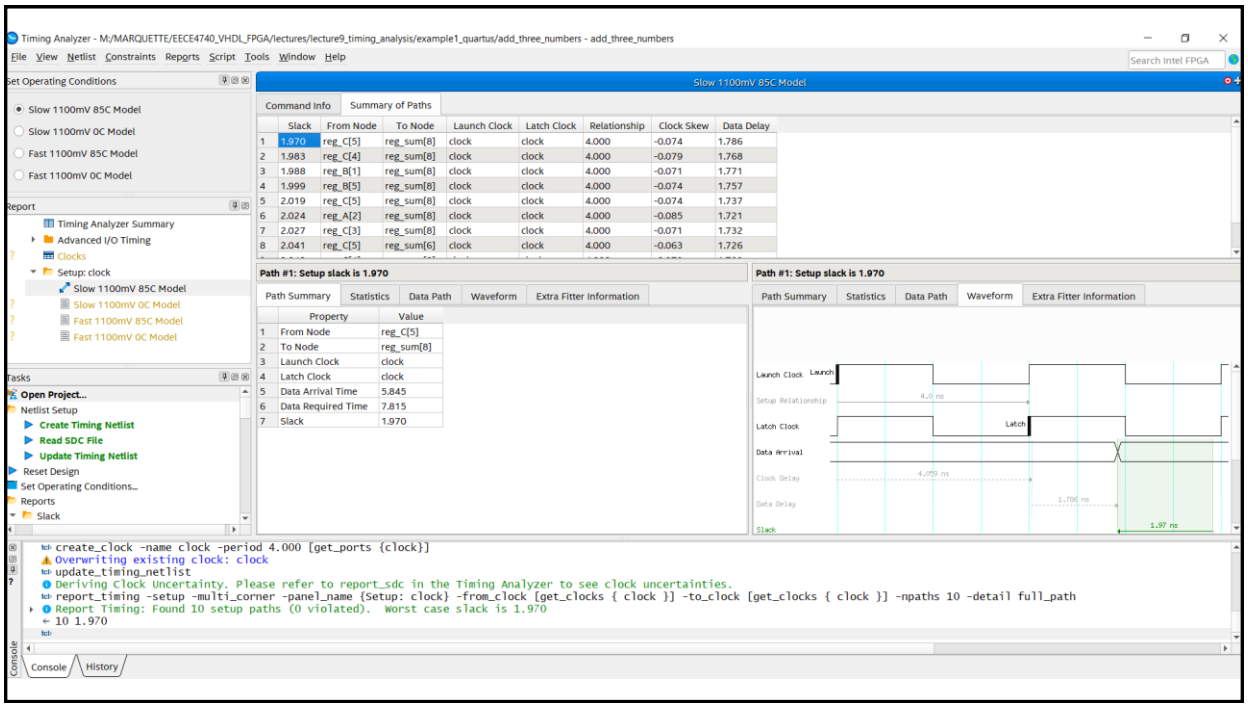

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Setting Up Timing Constraints for a Design – then, Recompile Design

- Close TimeQuest GUI
- Edit settings to include .sdc constraints file.
- In Quartus, recompile the design to see the effect of the new timing constraint on the compilation results.
- Then, follow the steps described previously to perform a new timing analysis using TimeQuest.
- The 4 ns timing constraint will cause the Quartus Prime optimization algorithms to make different decisions from those made when the (default) 1 ns constraint was used.
- In particular, the optimization algorithms will likely take less time to execute, because once the generated circuit has sufficient positive slack to meet the constraint, the algorithms can terminate.
- Next slides shows the results of timing analysis, with a positive slack of 1.734 ns.

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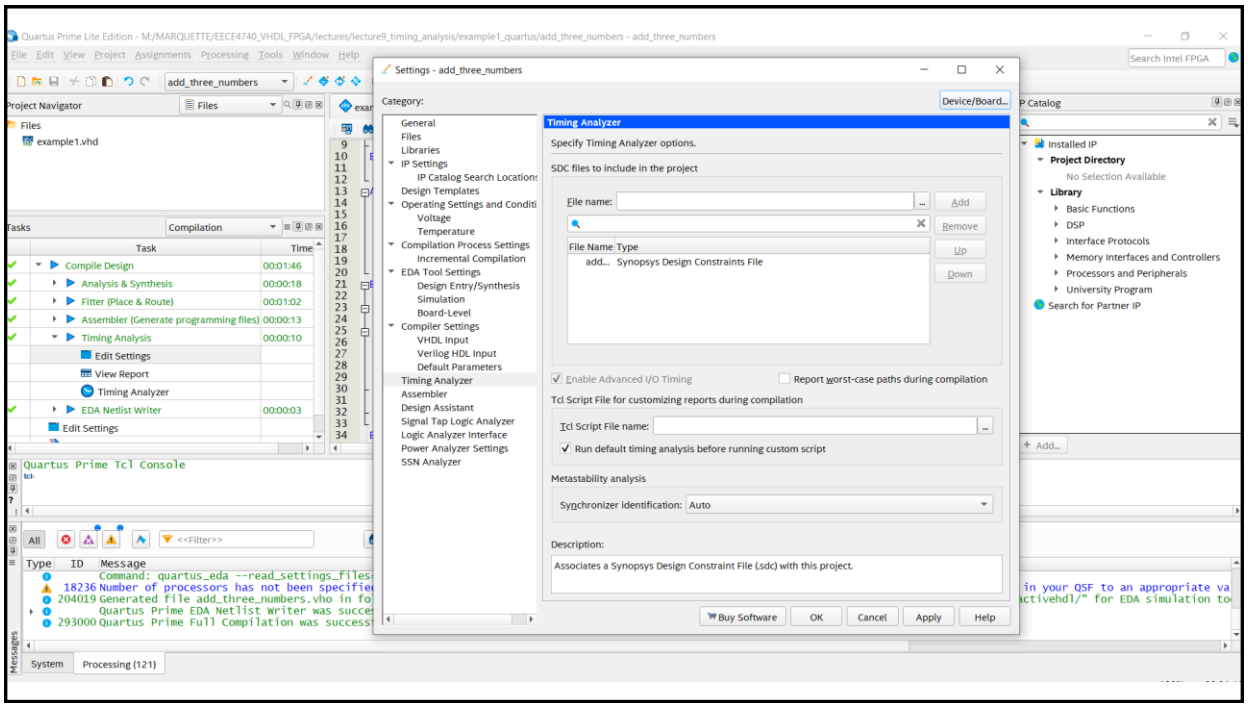
Settings - add_three_numbers
Timing Analyzer
Specify Timing Analyzer options.
SDC files to include in the project
Tcl Script File for customizing reports during compilation
Metastability analysis
Description:
Associates a Synopsys Design Constraint File (sdc) with this project.
Quartus Prime Tcl Console

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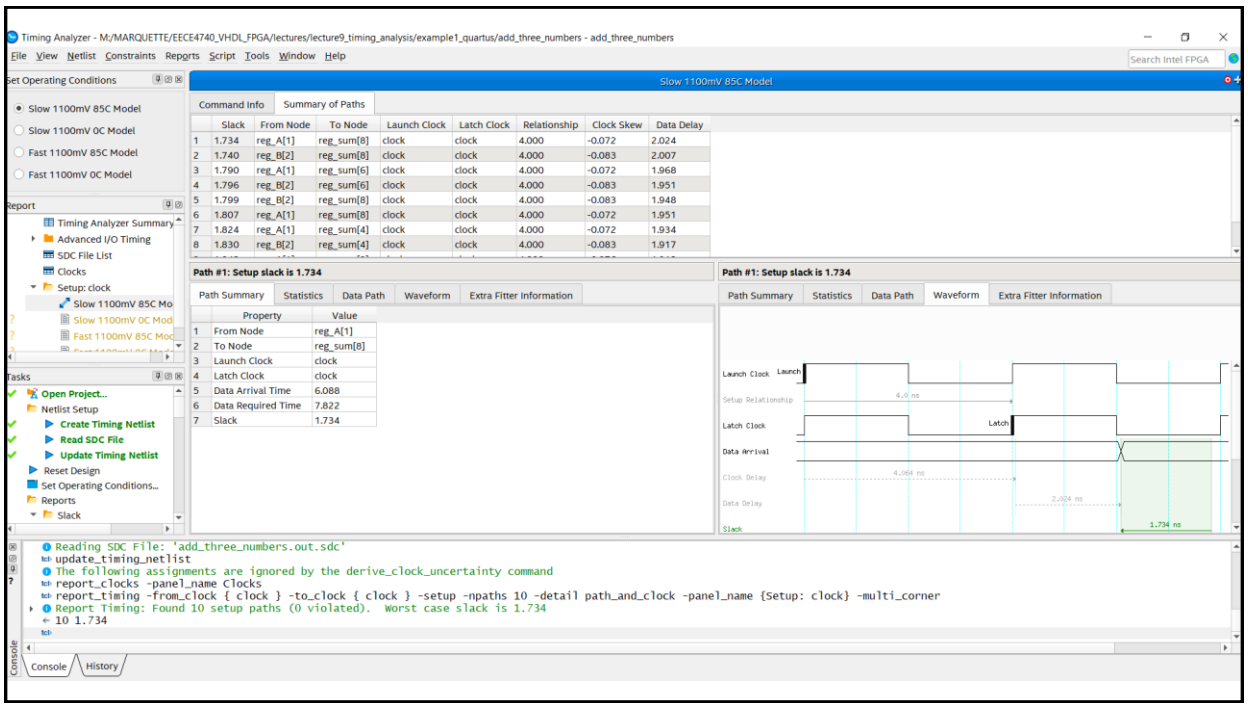
Timing Analyzer - M:/MARQUETTE/EECE4740_VHDL_FPGA/lectures/lecture9_timing_analysis/example1_quartus/add_three_numbers - add_three_numbers
Slow 1100mV 85C Model
Command Info
Summary of Paths
Path #1: Setup slack is 1.734
Path Summary
Statistics
Data Path
Waveform
Extra Fitter Information
Reading SDC File: 'add_three_numbers.out.sdc'
update_timing_netlist
The following assignments are ignored by the derive_clock_uncertainty command
report_clocks -panel_name Clocks
report_timing -from_clock { clock } -to_clock { clock } -setup -npaths 10 -detail path_and_clock -panel_name {Setup: clock} -multi_corner
Report Timing: Found 10 setup paths (0 violated). Worst case slack is 1.734
10 1.734

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Scenario #2
Typical sequential circuit (edge_detection_top_level.vhd)

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Setting Timing Constraints by Directly Editing add_three_numbers.out.SDC File

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```
#*************************************************************
# Time Information
#*************************************************************

set_time_format -unit ns -decimal_places 3

#*************************************************************
# Create Clock
#*************************************************************

create_clock -name {clock} -period 4.000 -waveform { 0.000 2.000 } [get_ports {clock}]
```

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Resources

- Quartus Prime Timing Analyzer Cookbook (27 pages)
  - https://www.intel.com/content/dam/www/programmable/us/en/pdfs/literature/manual/mnl_timequest_cookbook.pdf
- SDC Basics
  - https://www.vlsi-expert.com/2011/02/synopsys-design-constraints-sdc-basics.html
- SDC Commands
  - https://docs.verilogtorouting.org/en/latest/vpr/sdc_commands/

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Scenario #3
Simple combinational circuit (fourbit_adder.vhd)

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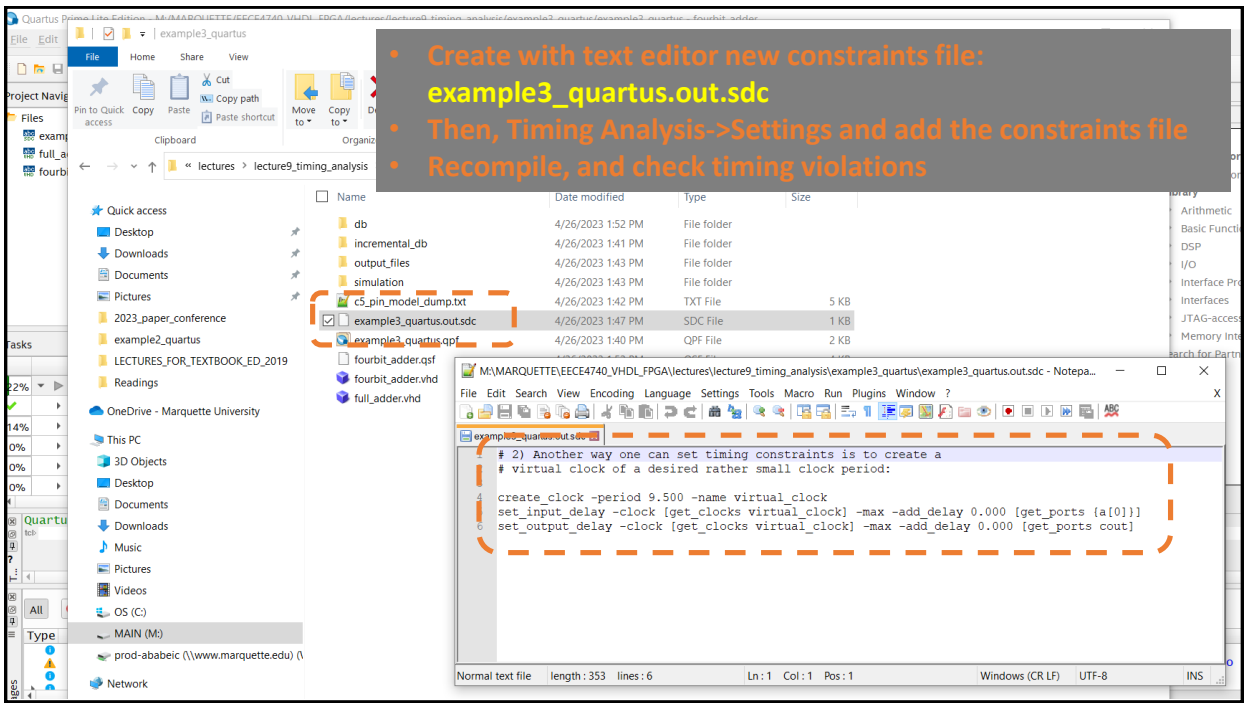

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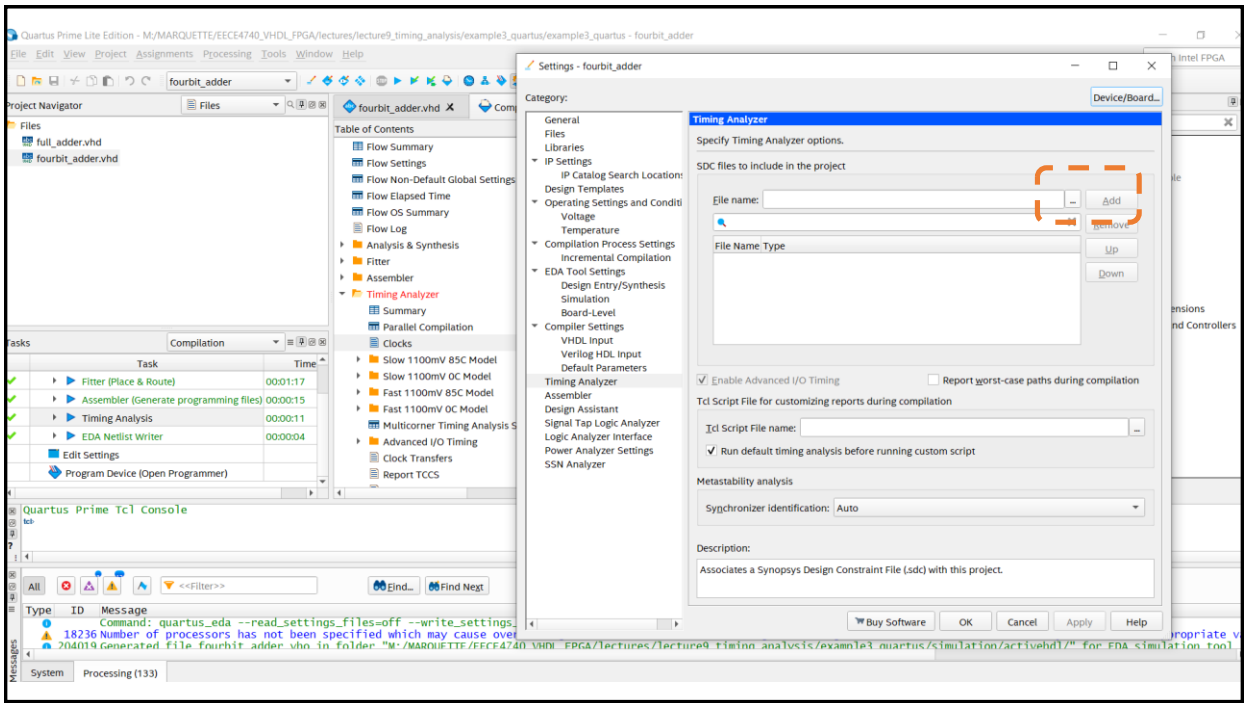
Settings - fourbit_adder
Timing Analyzer
Specify Timing Analyzer options.
SDC files to include in the project
File name:
Add
Remove
Up
Down
File Name Type
Enable Advanced I/O Timing
Report worst-case paths during compilation
Tcl Script File for customizing reports during compilation
Tcl Script File name:
Run default timing analysis before running custom script
Metastability analysis
Synchronizer identification: Auto
Description:
Associates a Synopsys Design Constraint File (.sdc) with this project.
Buy Software
OK
Cancel
Apply
Help

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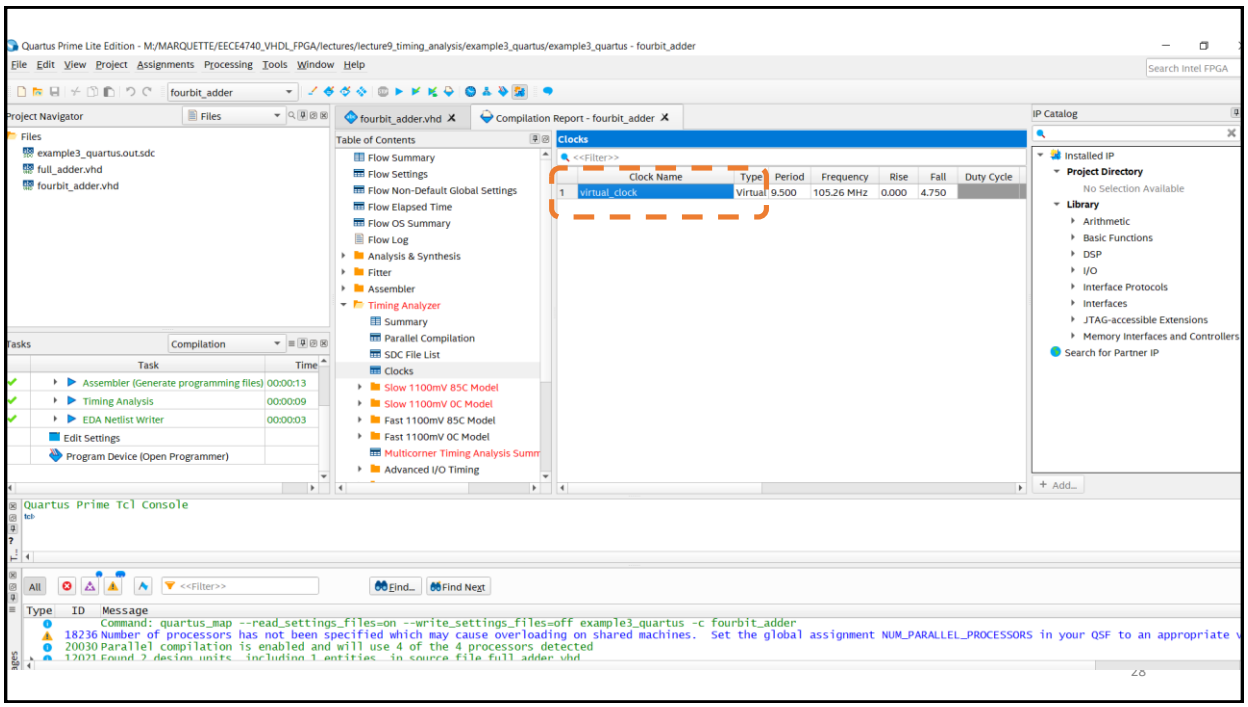
Clocks
Clock Name
Type
Period
Frequency
Rise
Fall
Duty Cycle
virtual_clock
Virtual
9.500
105.26 MHz
0.000
4.750
IP Catalog
Installed IP
Project Directory
Library
Arithmetic
Basic Functions
DSP
I/O
Interface Protocols
Interfaces
JTAG-accessible Extensions
Memory Interfaces and Controllers
Search for Partner IP

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References

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- https://www.intel.com/content/www/us/en/support/programmable/support-resources/design-examples/quartus/sof-qts-timinganalyzer.html
- https://www.intel.com/content/www/us/en/developer/topic-technology/fpga-academic/materials.html#hardwaredesign
- https://fpgacademy.org/tutorials.html
- https://siddharth.pro/2018/10/06/uart-achieving-timing-closure.html
- https://www.intel.com/content/www/us/en/docs/programmable/683588/17-1/quick-start-tutorial.html
- https://www.youtube.com/watch?v=HMAqjjCuDEI
- https://www.youtube.com/watch?v=bFmTHLZ3DGs
- https://www.youtube.com/@IntelFPGA/videos

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