entity fourbit_adder is
  end fourbit_adder;

architecture my_structure of fourbit_adder is
  component signals declarations
  begin
    port maps, etc.
  end my_structure;

-- this is a comment! because it starts with "--"
- component declarations
- signal declarations ←
- port map [example?]

b_adderP: FULL-ADDER port map (a(0), b(0), c0, z(0), c1);

"visualization" of port map:

Next time:
- You must read VHDL introduction (see website of class)
- We'll discuss FSM's in VHDL