

The following pseudo-code illustrates the behavior of the bit difference calculator. If there are X more 1's than 0's at the input, then the output is X. If there are Y more 0's than 1's, then the output is -Y.

```

Inputs: go, input (arbitrary width)
Outputs: output(arbitrary width), done (1 bit)

while (go == 0);
value = input; // Store input in a register called value.
                // This ensures that the code will still
                // work if input changes during the following
                // loop.

diff = 0;
for width iterations {
    if bit0 of value == 1
        diff++;
    else
        diff--;
    value = shiftRight(value,1);
}
output = diff;
done = 1;

```

One possible FSM (used by the FSM architecture in the VHDL):

