

EECE-4740, EECE-5740: Advanced VHDL and FPGA Design

Syllabus - 2018

Course info

EECE-4740, EECE-5740: Advanced VHDL and FPGA Design, 3 credits

Prerequisites: EECE-2030, EECE-3015.

Lecture: TueThu, 9:30-10:45am in Haggerty Hall, Room 388

Course webpage on D2L: <http://d2l.mu.edu>

Instructor

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Office hours: TueThu 8:30-9:30am or by appointment

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Course description

Present the background, abstractions, and techniques for advanced digital circuits design and optimization. Emphasis is placed on specification and synthesis using VHDL and on prototyping using FPGAs of complex systems. Such systems represent examples from various application domains, including processors, image and video processing, filtering and other DSPs, and power electronics.

Textbook

Research papers, lecture notes, and other teaching materials will be distributed during classes. No specific textbook is required.

Course objectives

By the end of this course students should be able to perform the following tasks:

1. Describe Field Programmable Gate Array (FPGA) technologies.
2. Describe typical design methods of digital circuits implemented as FPGA circuits.
3. Utilize VHDL to specify complex circuits and synthesize these circuits with CAD tools (e.g., Altera and/or Xilinx tools).
4. Describe and utilize simulation tools for measuring and reporting performance of complex digital systems.
5. Conduct experiments using an evaluation board to confirm the analysis done in class.
6. Prepare informative and organized written and video reports that describe the methodologies employed, the results obtained, and the conclusions made in simulation and hardware experiments.
7. Prepare review-type reports of selected technical research articles.

Course policies

Grading: Grading is based on the following components:

- Paper presentations and in-class participation: 20%
- Homework assignments: 40%
- Several implementation projects: 40%

Grading scale:

A [94-100]%; A- [90-94]%; B+ [87-90]%; B [83-87]%; B- [80-83]%; C+ [77-80]%; C [73-77]%; C- [70-73]%; D+ [67-70]%; D [60-67]%; F [0-59]%.

Homework policy: All assignments are due at the beginning of class unless otherwise specified. Late submissions will not be accepted. If you are absent from class or you know that you will be absent from class, you should as soon

as possible arrange with the instructor for any missed work. It is the student's responsibility to contact the instructor in such a case. Arrangements made in advance of an absence (if approved) may allow full credit to be given for late work. Include your name only (no MUID) on all homework assignments, reports, exams, etc. Turn in solutions that are written clearly and neatly; turning in disorganized or esthetically-ugly solutions with scratched-out text, figures, and formulas, etc. is penalized by deducting grade-points even if the final answer is correct.

Attendance: Attendance is required, per engineering and university policies at:

<http://bulletin.marquette.edu/undergrad/academicregulations/#attendance>

There is no penalty for excused absences (must be pre-approved). After two unexcused absences, the final grade may be lowered by 2 percentage points per additional absence. Excessive absences (i.e., when more than 6 classes have been missed) may result in being dropped from the course. In addition, all students must attend the Design Day in the College of Engineering, on the last day of classes.

Class participation: You are expected to pro-actively participate in this course. Active participation means to study the assigned reading items before class, ask and answer questions, and participate in discussions during lectures. Proactive participation means to search and read – on your own – additional information (e.g., online articles, research papers, textbooks, etc.) related to the topics of this course and to share it with the other students and the instructor during outside or in class discussions.

Academic integrity: All submitted work should be your own. Instances of plagiarism and cheating will result in all students involved getting an automatic zero on the assignment/exam/project and potentially a failing grade based on the severity of the case. Please refer to the Marquette University's Academic honesty policies and procedures:

<http://bulletin.marquette.edu/undergrad/academicregulations/#academichonestypolicy>

Special needs: If you have a disability and require accommodations, please contact your instructor early in the semester so that your learning needs may be appropriately met. You will need to provide documentation of your disability to the Office of Disability Services (OSD). If you are unsure of what you need to qualify for services, visit the OSD website at <http://www.marquette.edu/disability-services/forms.shtml> or contact the Office of Disability Services at 414-288-1645. The Office of Disability Services is in Marquette Hall 05.

Usage of media and electronic devices: Usage of cell phones, laptops, tablets, newspapers, magazines, etc. is not allowed during lectures unless instructed to do so by the instructor.

Paper presentations and discussions

Students will be required to read assigned technical research papers, to discuss, and to make in-class presentations. Each student will make one individual presentation and will be expected to participate in all paper discussions.

Projects

There will be several projects, which will require students to implement the components of a complex digital system using VHDL and FPGAs.

Graduate students

Graduate students enrolled in this course are expected to work on significantly more difficult project topics. In addition, graduate students may be required to work individually, as opposed to working in teams, on selected projects.

Outline

1. Introduction
2. Field Programmable Gate Array (FPGA) technologies
3. VHDL concepts and programming
4. Design methods for FPGA circuits
5. Specification, synthesis, and FPGA implementation of selected complex systems, e.g. digital camera, network-on-chip, video game, video encoders and decoders, processors, etc.