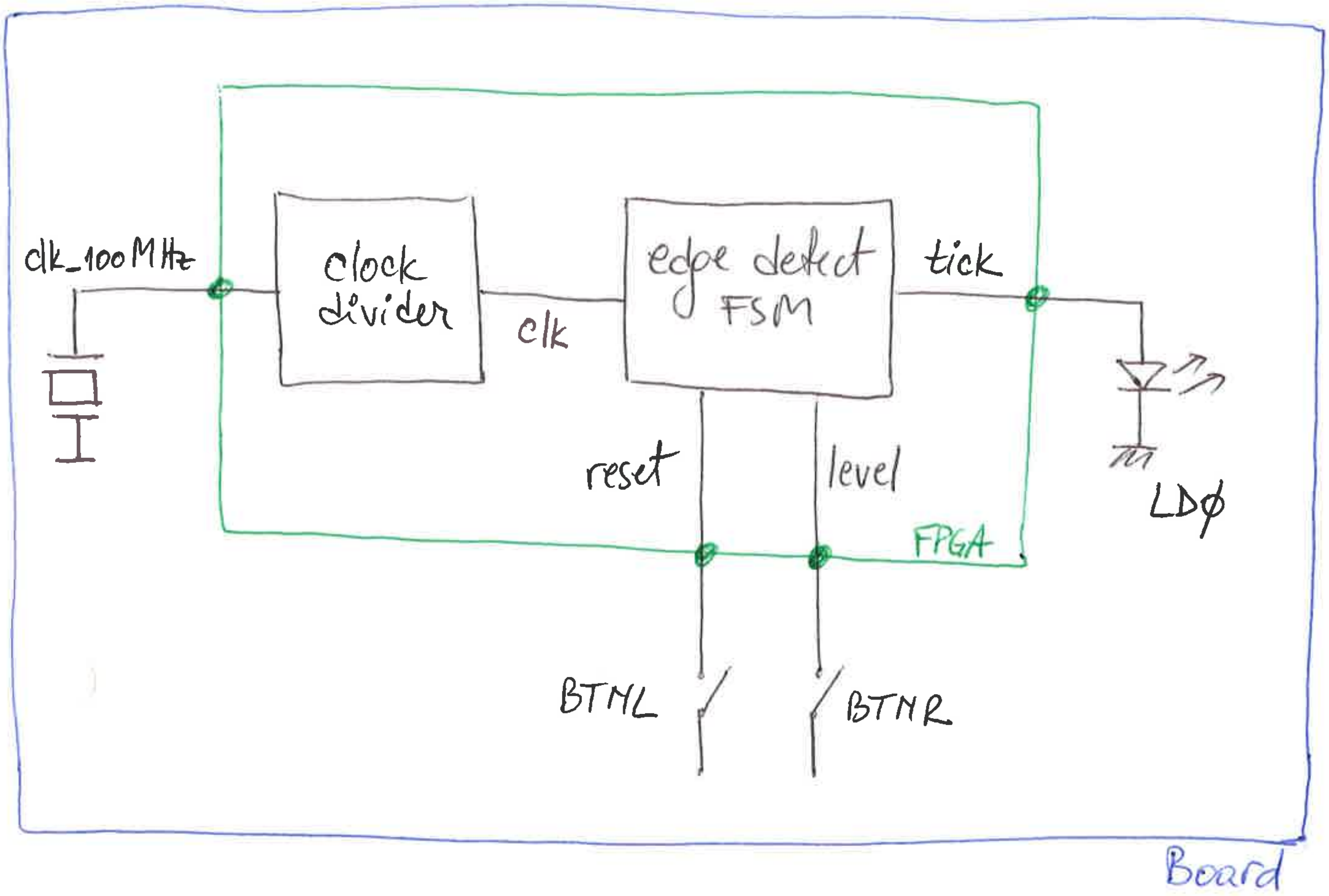
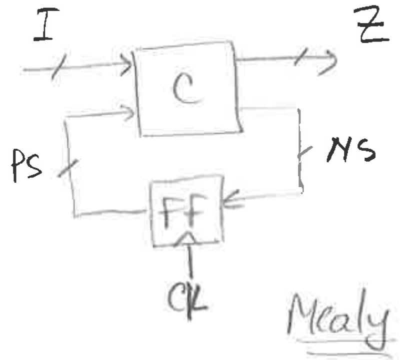
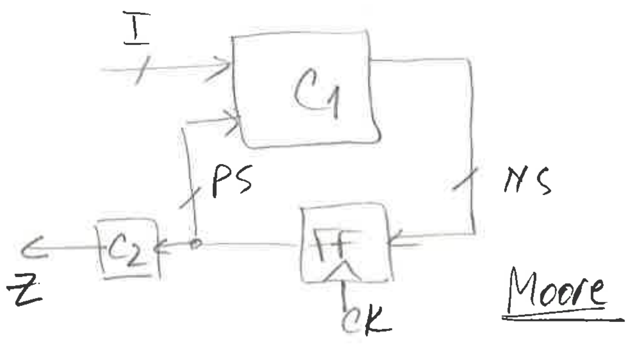
Edge detection circuit



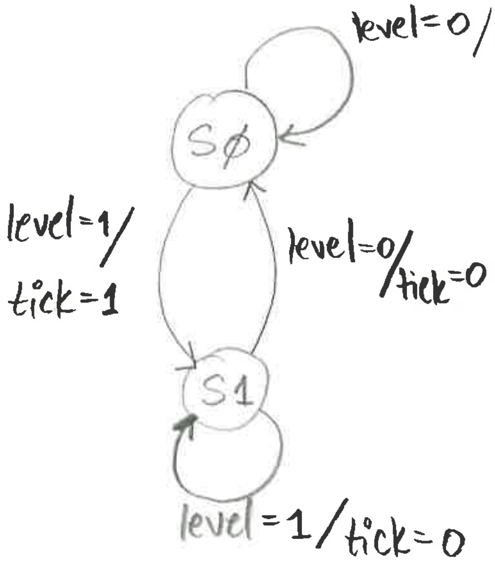
Finite State Machines (FSM) in VHDL

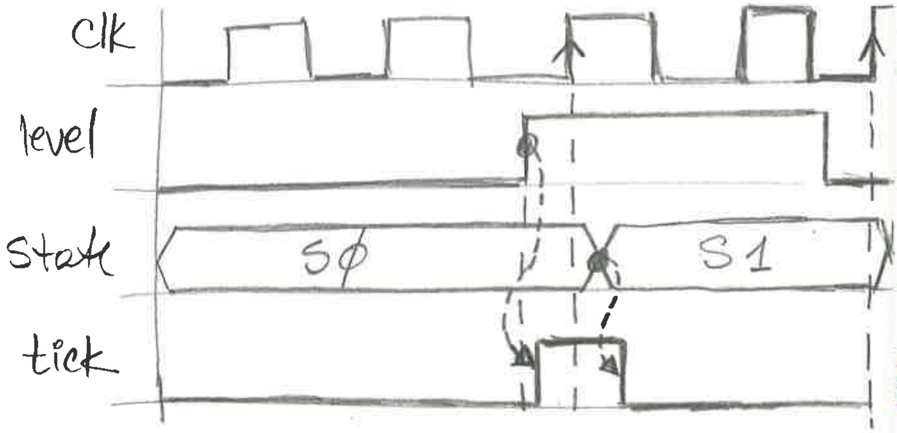
Sequential circuits are modeled as FSM's because they transit among a finite number of internal states.

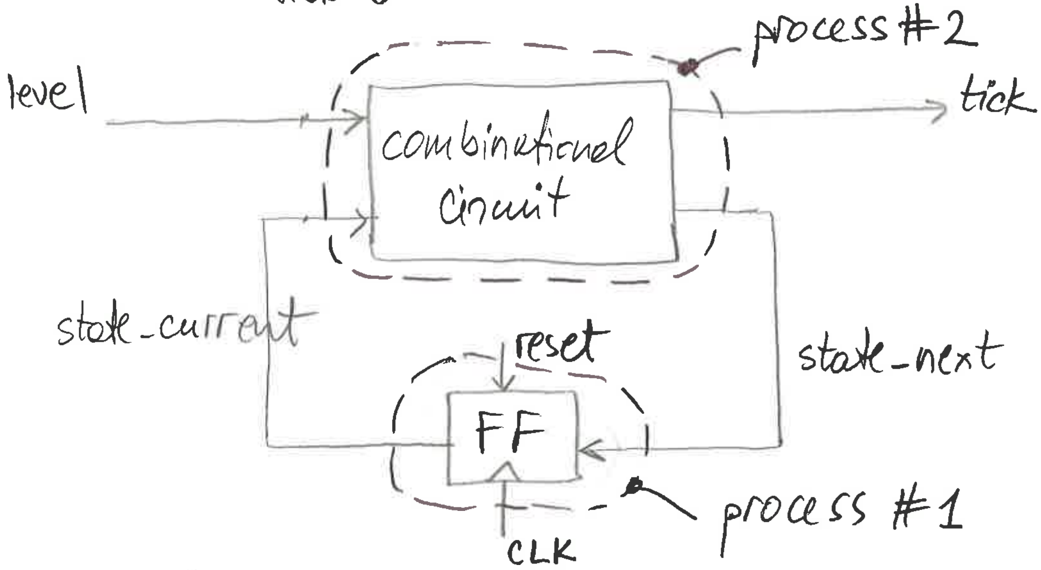




Example of Mealy machine : Edge detector of rising edges







VHDL description: "Two process model"

```
library ieee;
use ieee.std_logic_1164.all;

entity edge_detect is
    port ( clk, reset, level : in std_logic;
           tick : out std_logic);
end edge detect;

architecture MEALY_ARCH of edge_detect is
    type state_type ( S0, S1 );
    signal state_current, state_next : state_type;

    begin
      -- state register; process #1
      process (clk, reset)
      begin
            if (reset = '1') then
                  state_current <= S0;
            elseif (clk'event and clk = '1') then
              state_current <= state_next;          !
            end if;
      end process;
      -- next state and output logic; process #2
      process (state_current, level)
      begin
        state_next <= state_current;   } ?
        tick <= '0';
        case state_current is
            when S0 =>
                 if level = '1' then
                       state_next <= S1;
                       tick <= '1';
                 end if;
            when S1 =>
                 if level = '0' then
                       state_next <= S0;
                 end if;
        end case;
      end process;
end MEALY_ARCH;
```

describes how states are transitioned from one to another.

"imagine" them being executed concurrently.