Four Bit Binary Counter

We design a 4-bit binary counter. Our counter has an output "Q" with four bits. During correct operation, the counter starts at "0000" and then binary counts up to output "0001", "0010", "0011", and so on until it outputs "1111", after which it resets to "0000" and starts again. The implementation has only one input: a clock signal of 100MHz, generated by a clock generator outside the FPGA chip. We'll use the output Q to drive the first four LEDs on the FPGA board.

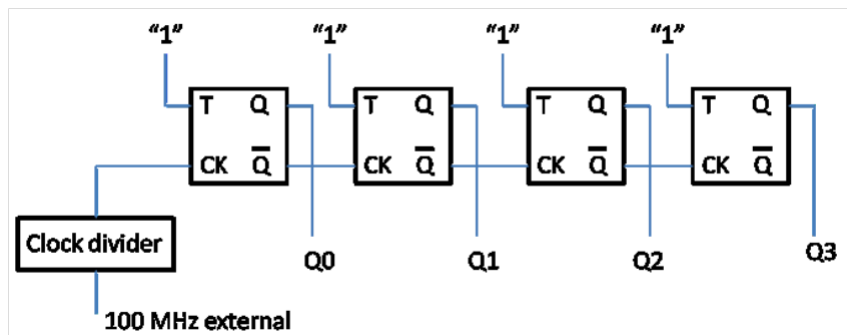The block diagram of the **structural description** of such a binary counter is shown in the next figure. This implementation is known as a ripple counter.

Figure 1 Block diagram of a 4-bit binary counter